CadMOS Design Technology, Inc.

Presents

Noise Analysis for IC Design

CadMOS
DESIGN WITH INTEGRITY

Company Introduction

- Privately held, founded in San Jose CA, Aug 1997
- 3 co-founders:
  - **Dr. Charlie Huang CEO**, Ex VP of R&D Synopsys/EPIC, originator of PowerMill, manager of PathMill
  - **Dr. Ken Shepard CTO**, Ex IBM Yorktown, G4 µP design lead, noise analysis expert
  - **Dr. Vinod Narayanan VP of R&D** , Ex IBM Yorktown, static noise analysis developer, static analysis expert
- $3m investment from venture capital (USVP) and other investors

Company Mission

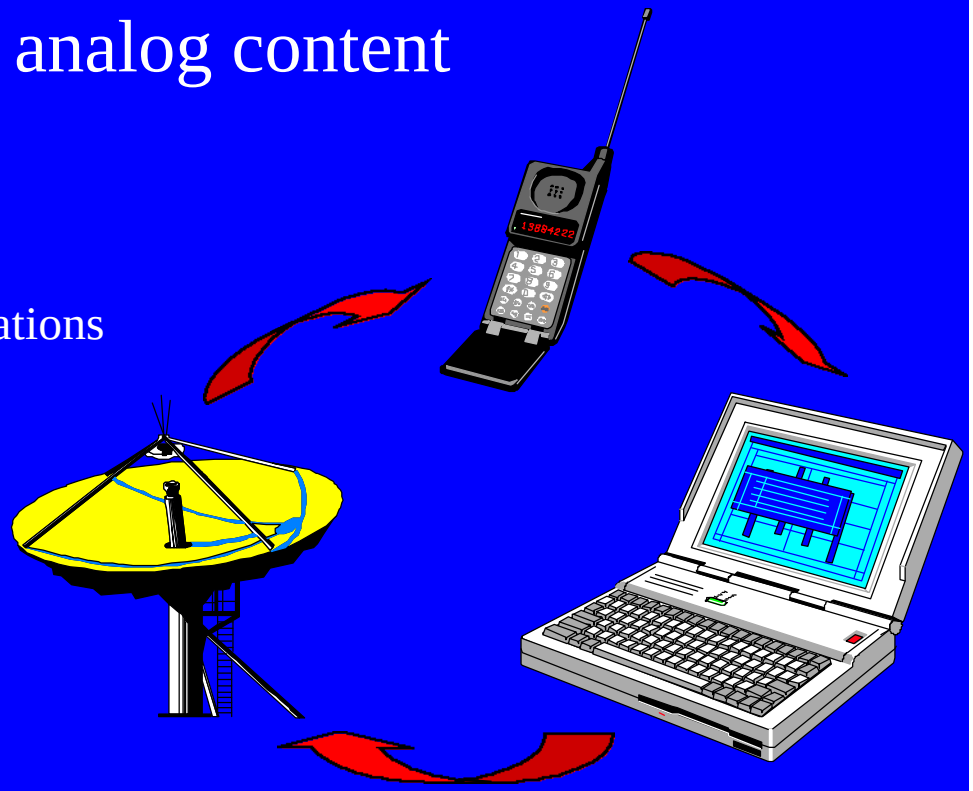
Provide premium solutions to noise, signal integrity, and other electrical problems in advanced leading edge designs

Company Status

- Current staff of 18 people (9 R&D)
- Production release of PacifIC, Dec 98
  - Static noise analyzer for digital ICs
  - First orders received in Q1 1999 from TI and AMD
- Acquired technology and R&D staff of Apres Technologies, Inc. in January 1999
  - Pioneers in mixed signal substrate noise analysis
  - New product SeismIC, alpha released May 1st 1999

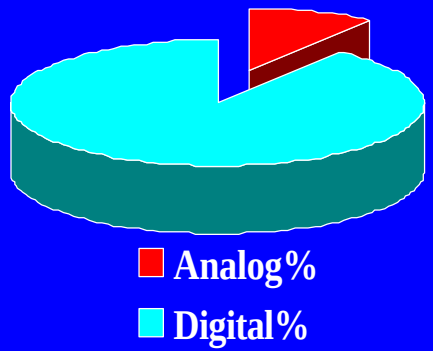
Mixed Signal Market

- Demand for fast, low cost, portable, wireless electronics is driving the need for “systems on silicon” with significant analog content
- Key growth areas are
  - Wireless
    - Cell phone handsets, Base Stations
  - Networking
    - xDSL, Modems
  - Disk Drives
  - Datacoms
  - Consumer

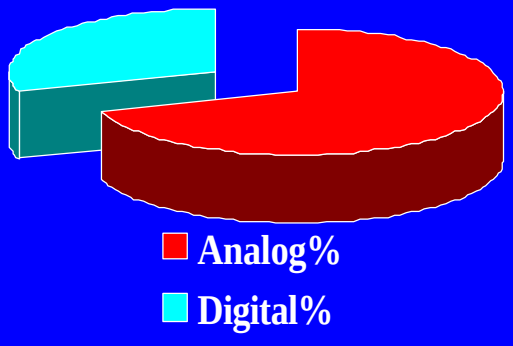


Mixed Signal Design Productivity

Transistor Counts



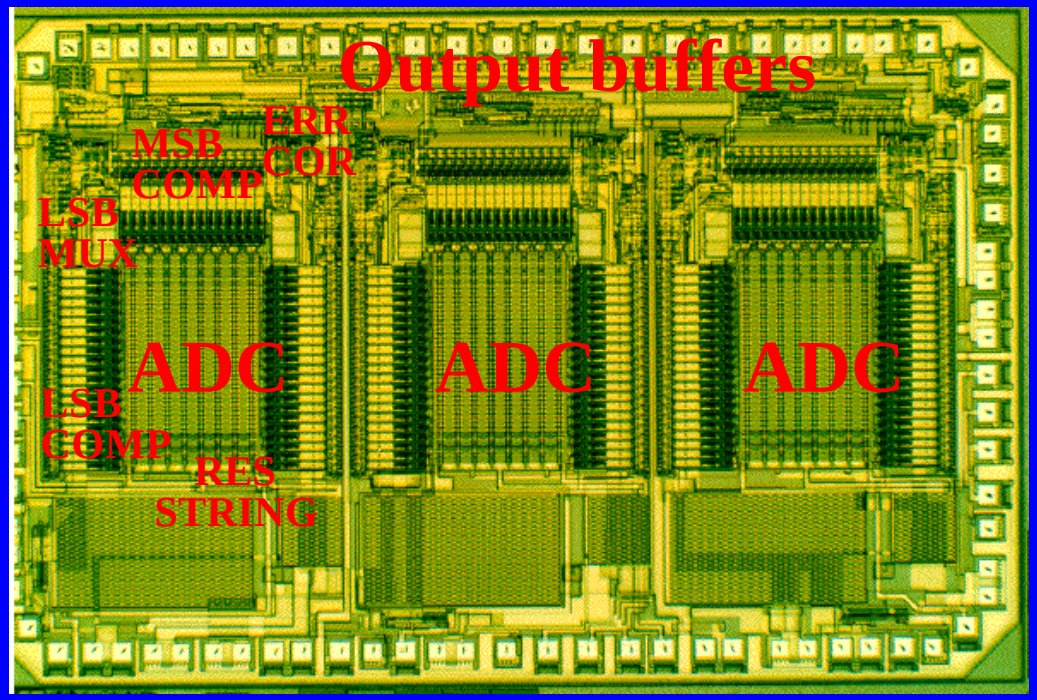
Design Time



Unwanted interactions between digital and analog circuitry is seriously limiting mixed-signal design productivity!

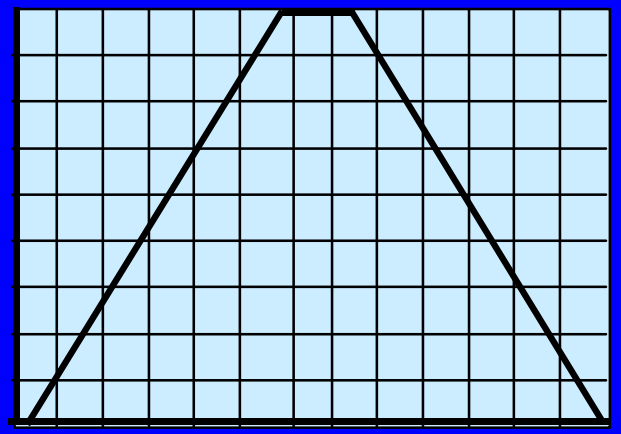
Source : Dataquest

Triple 8-b Video ADC



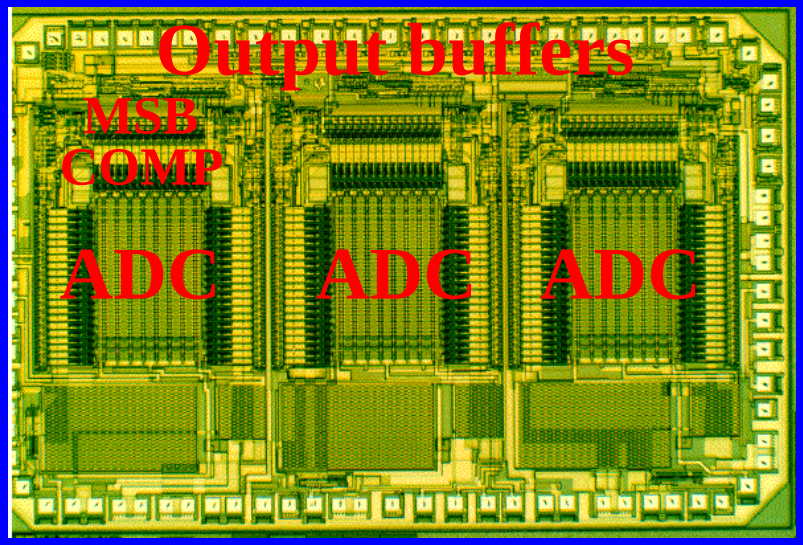
Resolution	**8b**
Power	**630mW**
Output Frequency	**20MHz**

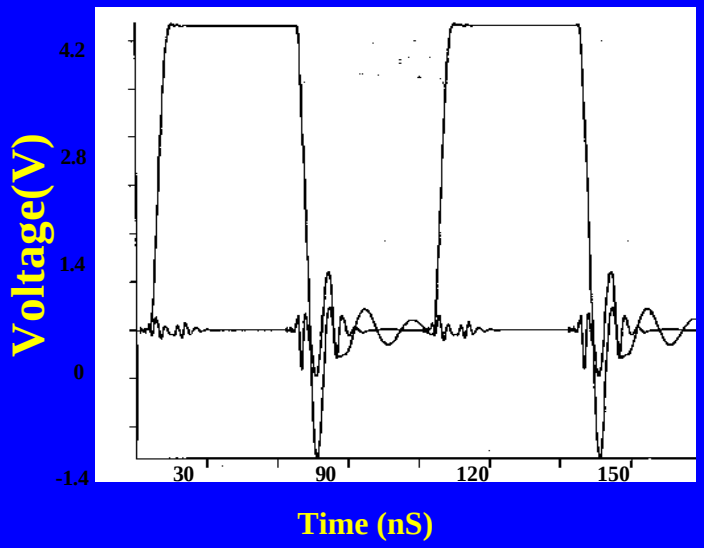
Expected response



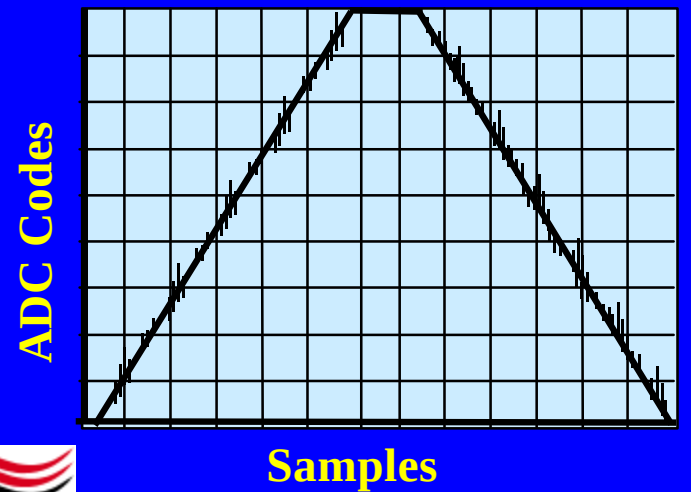
Noise Impact on ADC

Simultaneous switching of the output buffers creates noise during MSB comparisons



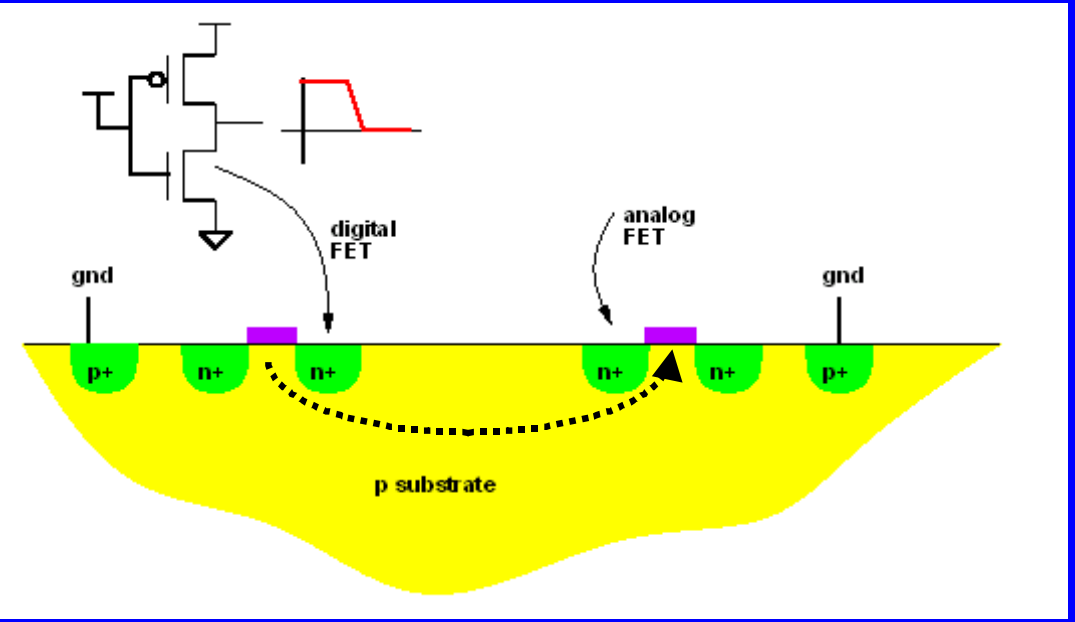


Actual response shows sparkle codes in ADC ramp



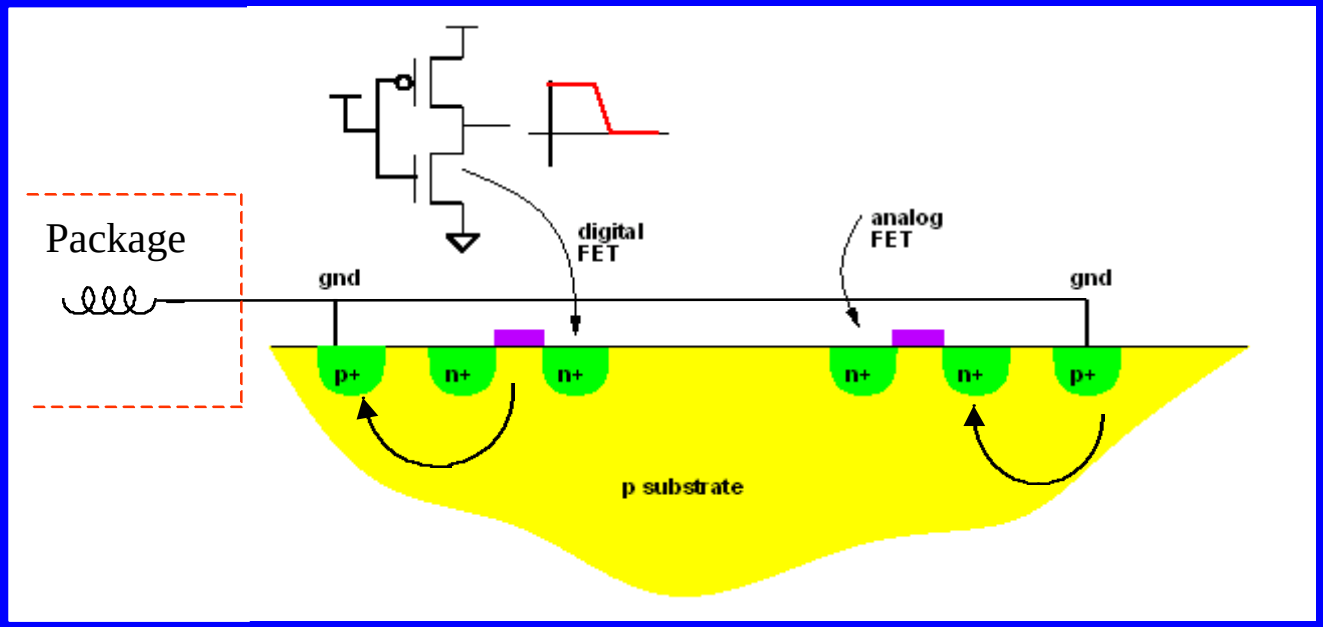
Noise in Mixed Signal ICs

- Substrate and Interconnect Noise :
  - switching currents from devices and interconnects coupled through substrate to sensitive analog devices



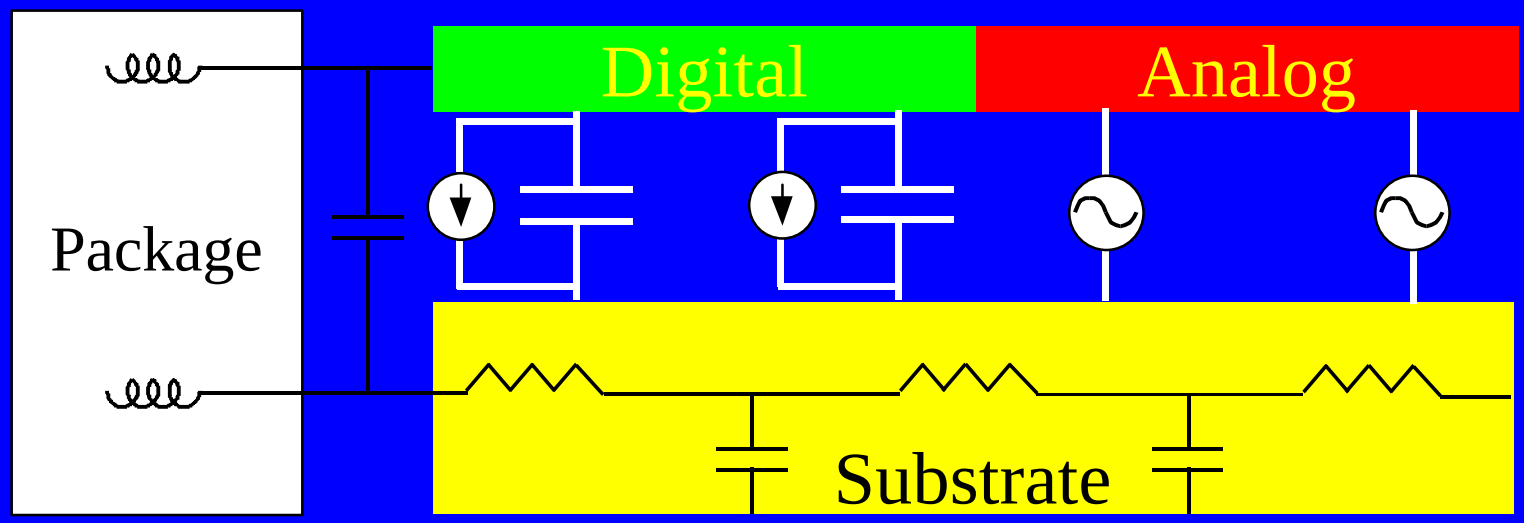
Noise in Mixed Signal ICs

- Supply/Package Noise :
  - Simultaneous switching of I/O buffers causes variations in the power supply due to package inductance
  - Noise from supply is coupled to analog devices through substrate contacts



Mixed-Signal Noise Analysis

- *Components of substrate noise*



CadMOS Design Technology, Inc.

Introduces

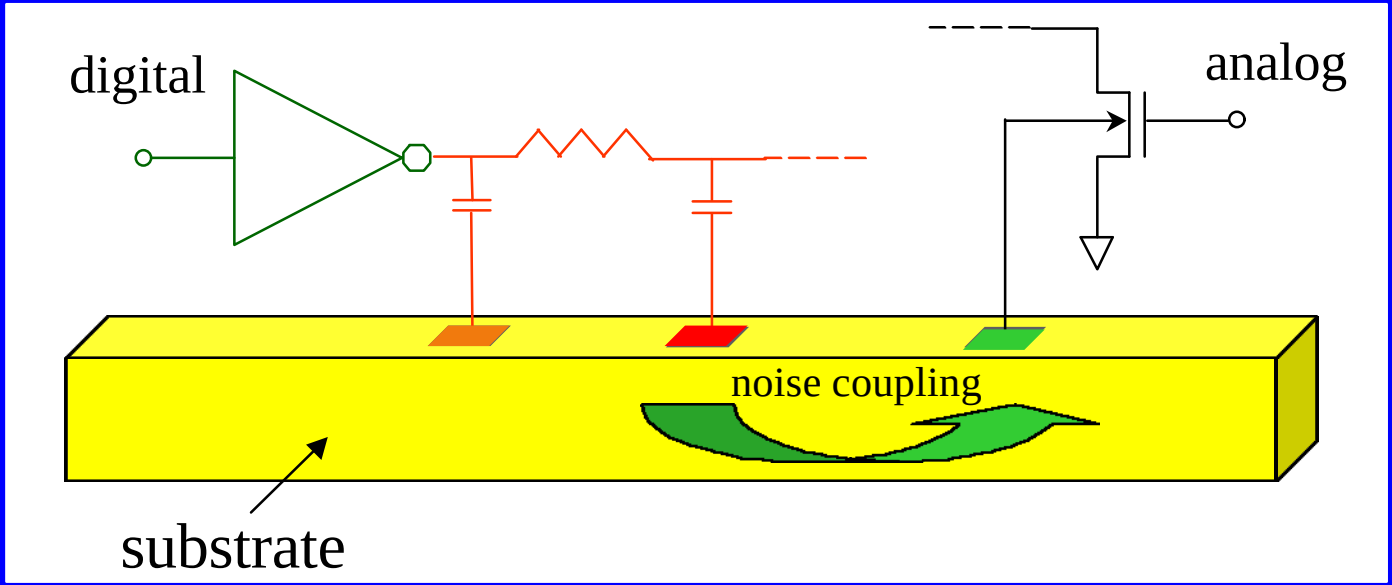
SeismIC

Noise Analysis for Mixed Signal ICs

CadMOS
DESIGN WITH INTEGRITY

SeismIC : Substrate Noise Analysis

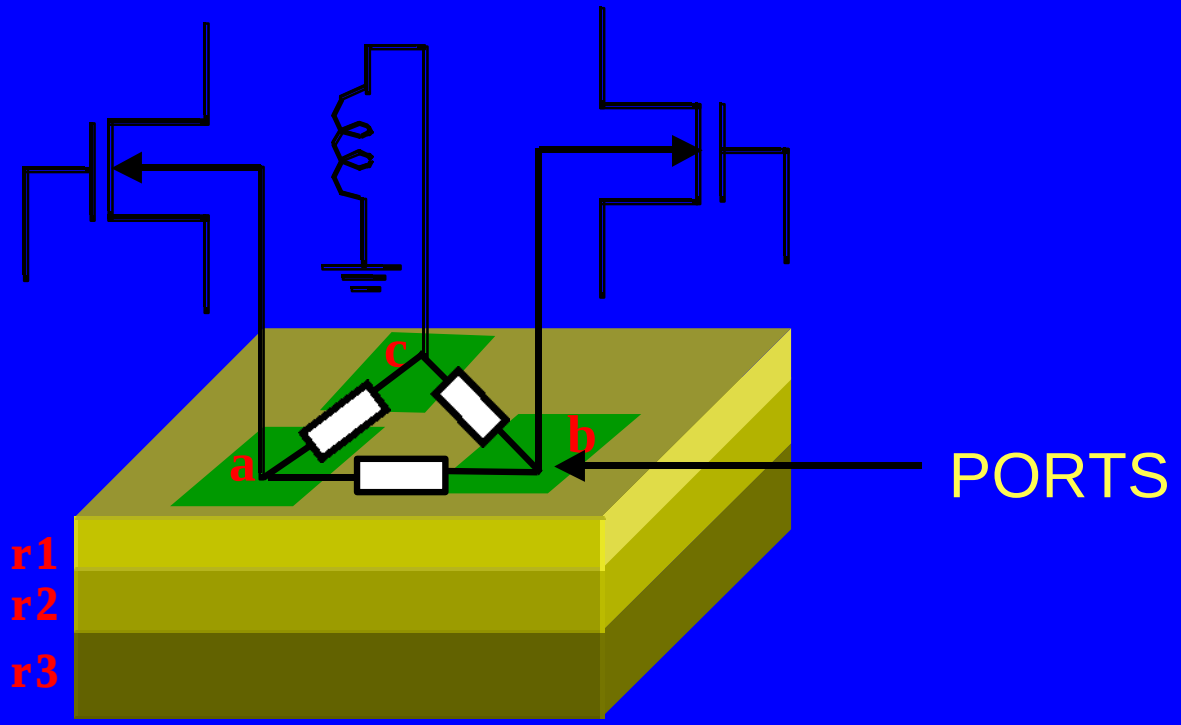
- Analyzes substrate/interconnect/package (SIP) noise in large mixed signal designs
- Highlights substrate noise on layout display



SeismIC - Substrate Noise Analyzer

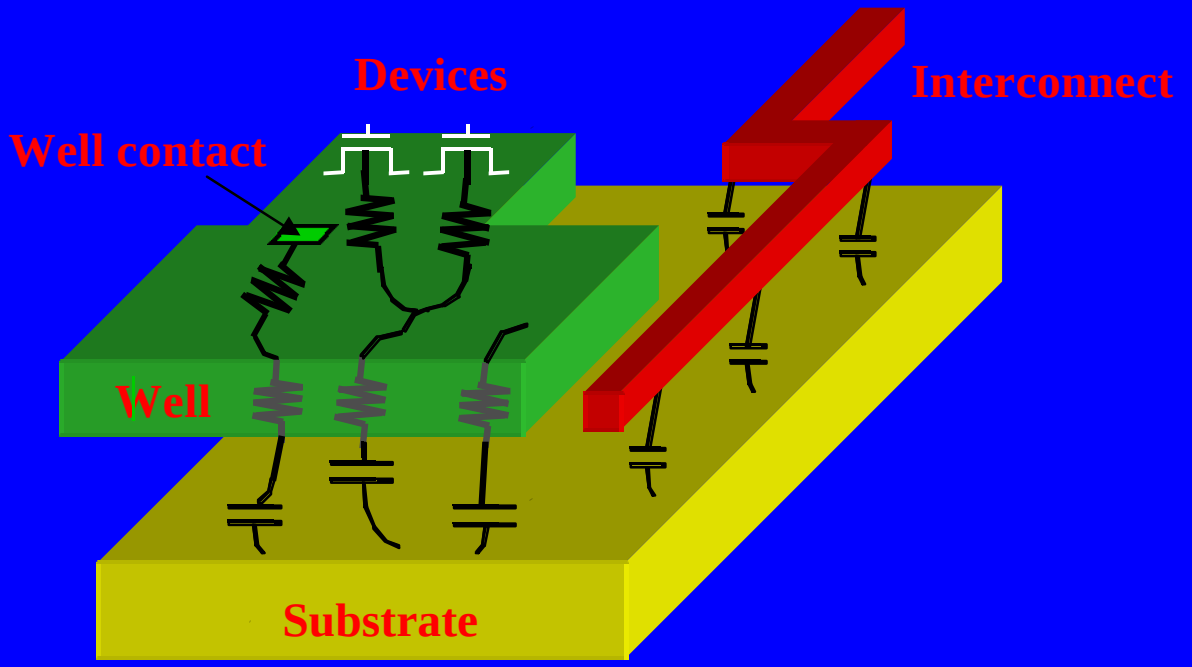
- Efficiently models full chip substrate
  - including BiCmos, twin-well, triple-well, standard CMOS
- Performs noise sensitivity analysis for critical analog transistors
  - identifies the major noise contributors attacking the critical devices
- Advises on the impact on noise of design changes
  - guard rings, layout, package, process etc.
- Creates simplified substrate noise model for circuit simulation

Modeling the Substrate



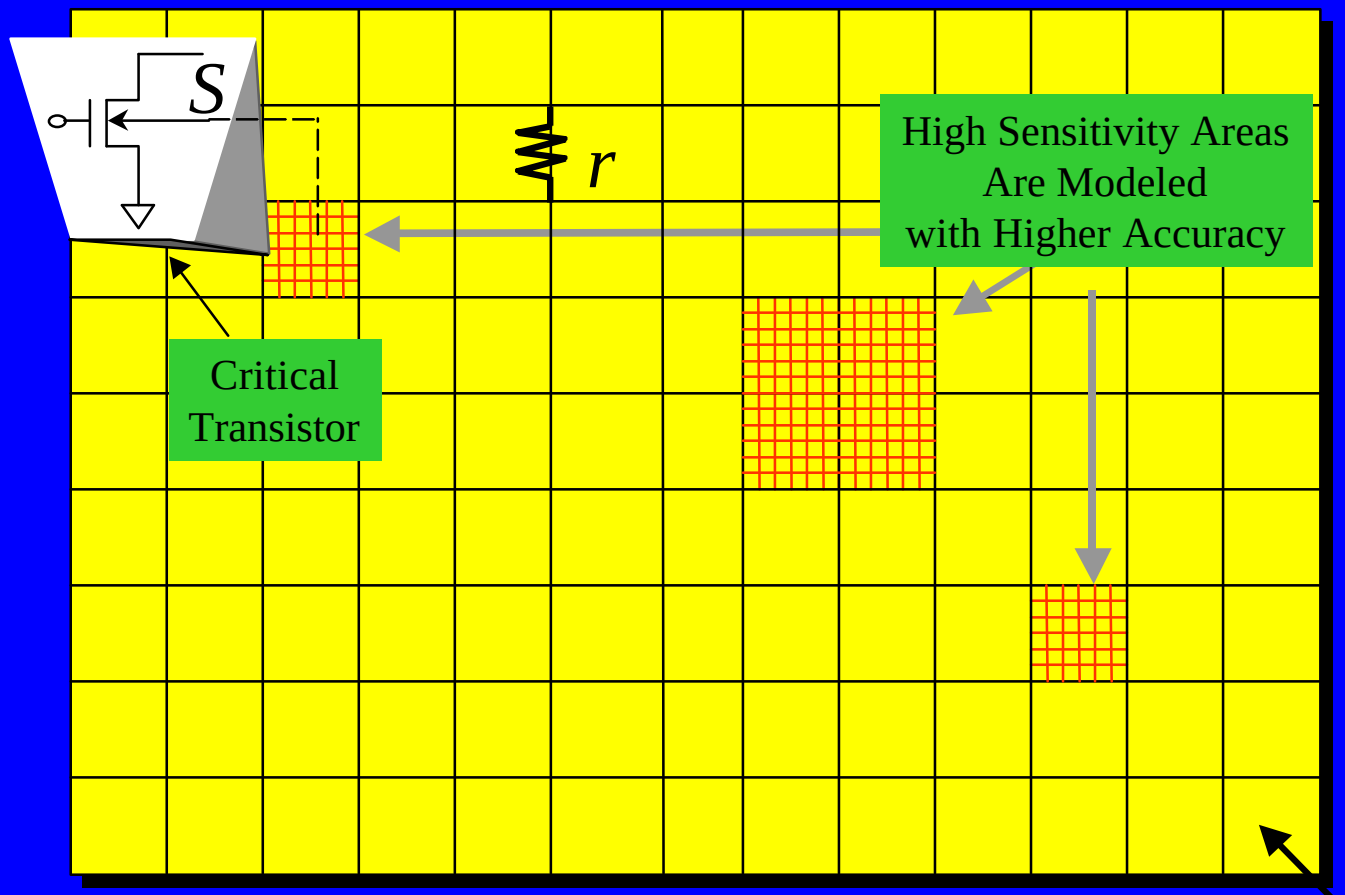
- Define ports on substrate that connect to circuit
- Extract port-to-port RC model of substrate

Modeling Wells / Interconnect



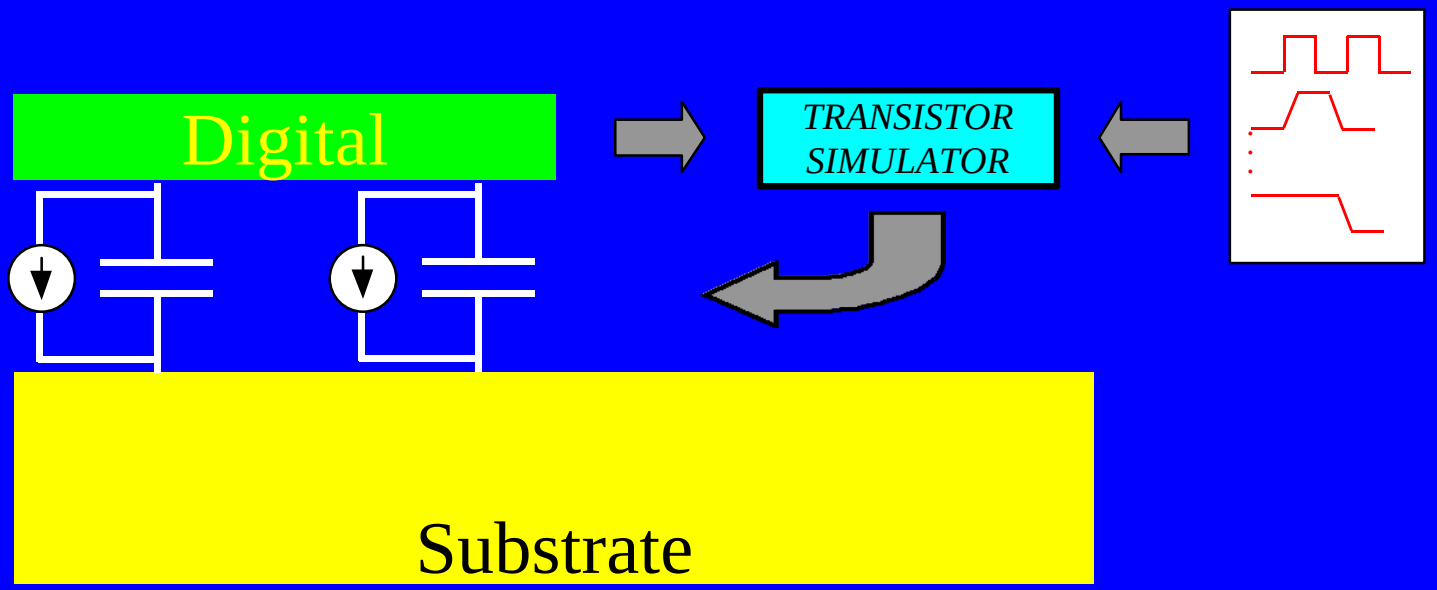
- Use extracted capacitance for interconnect
- Extract RC model for wells

Adaptive Substrate Modeling

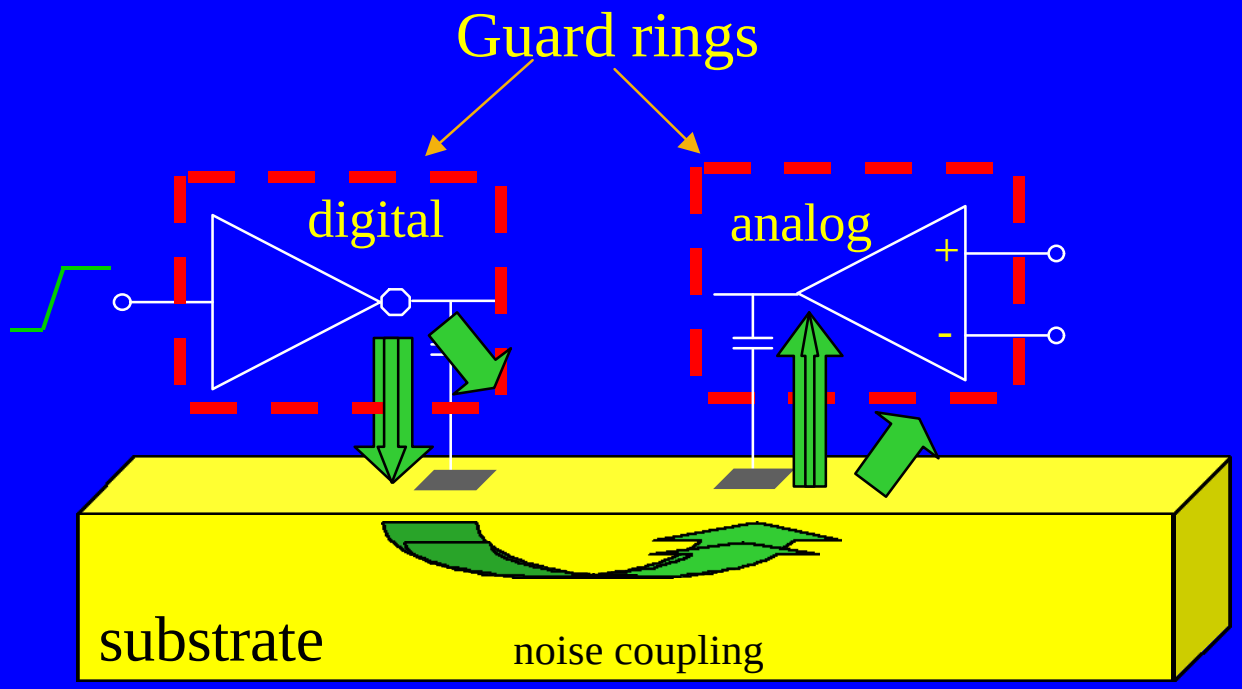


Modeling Switching Noise

- Model power supply and drain/source switching currents of digital transistors



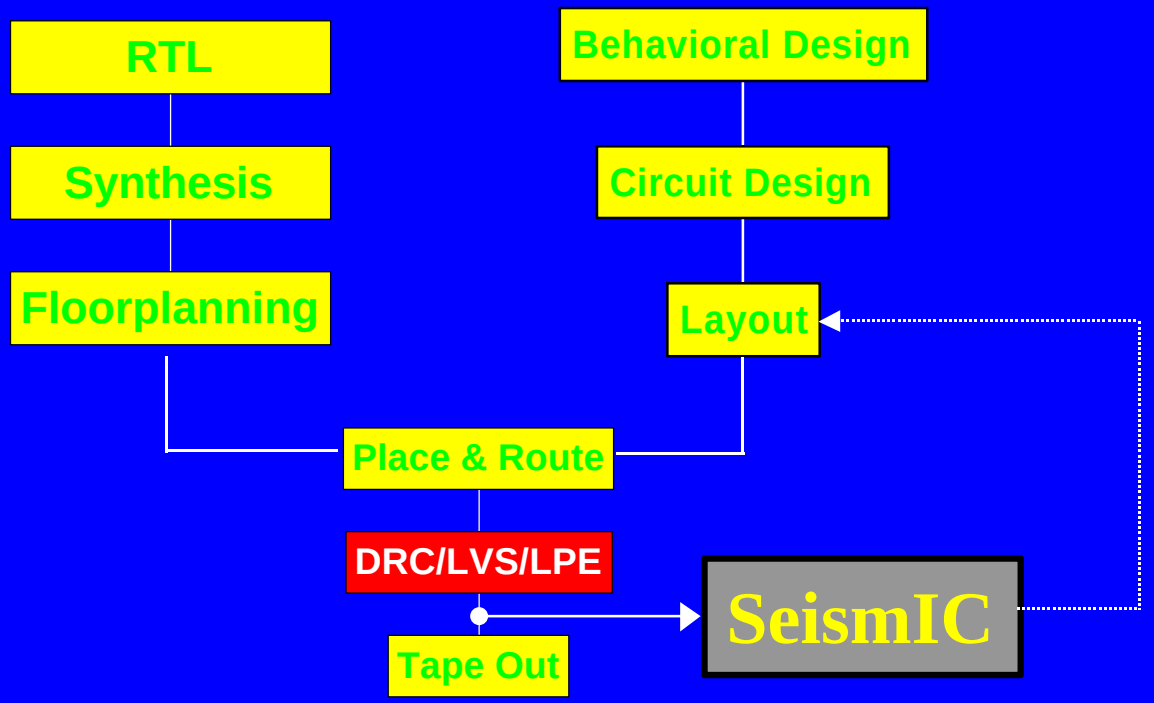
SeismIC - Advising on Guard Rings



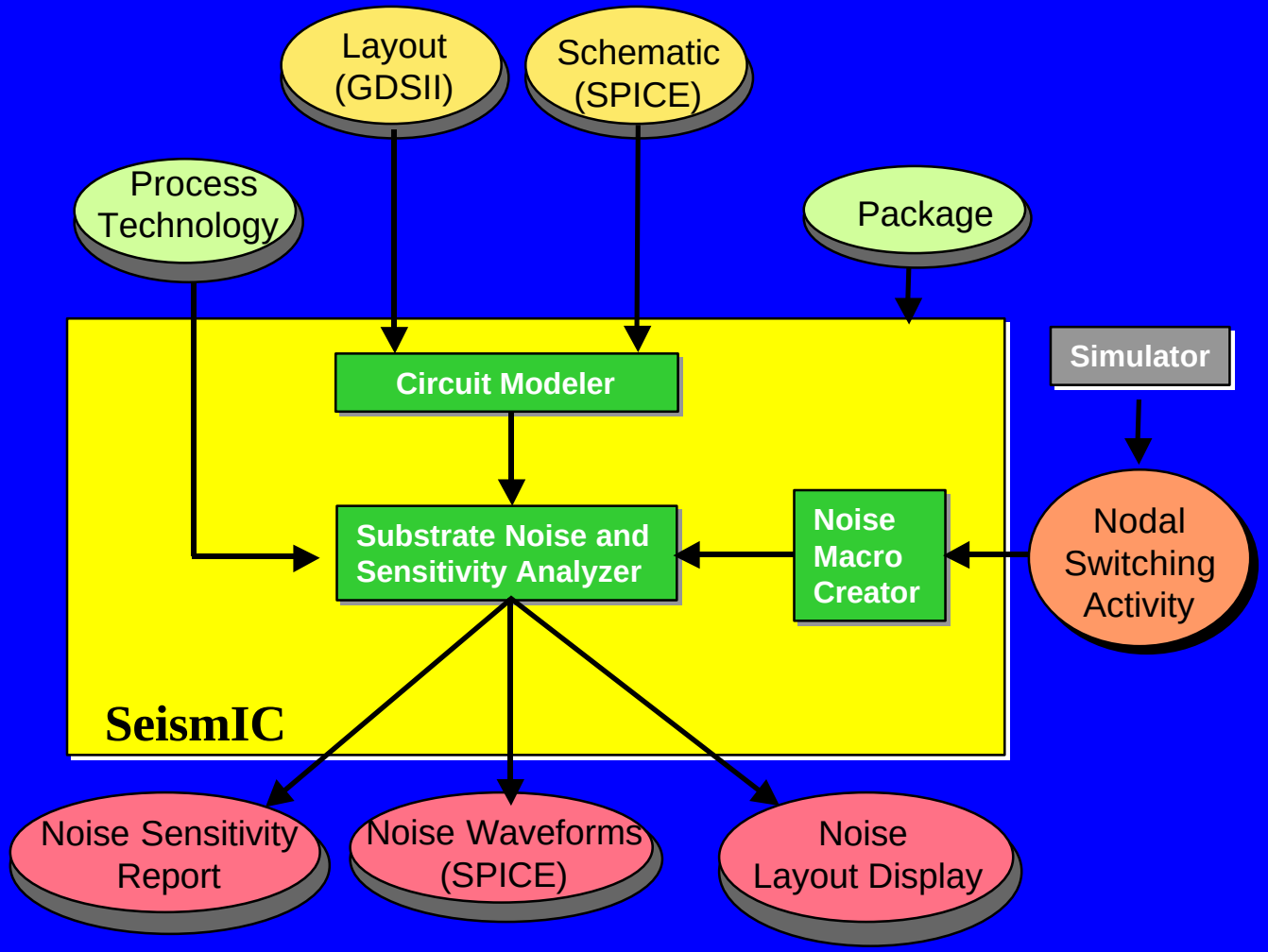
- SeismIC can determine the most effective use of guard rings to protect against substrate noise
  - In some cases guard rings may increase the noise at sensitive analog devices!

SeismIC in the Mixed-Signal Design Flow

Digital Design Flow Analog Design Flow



SeismIC : Data Flow



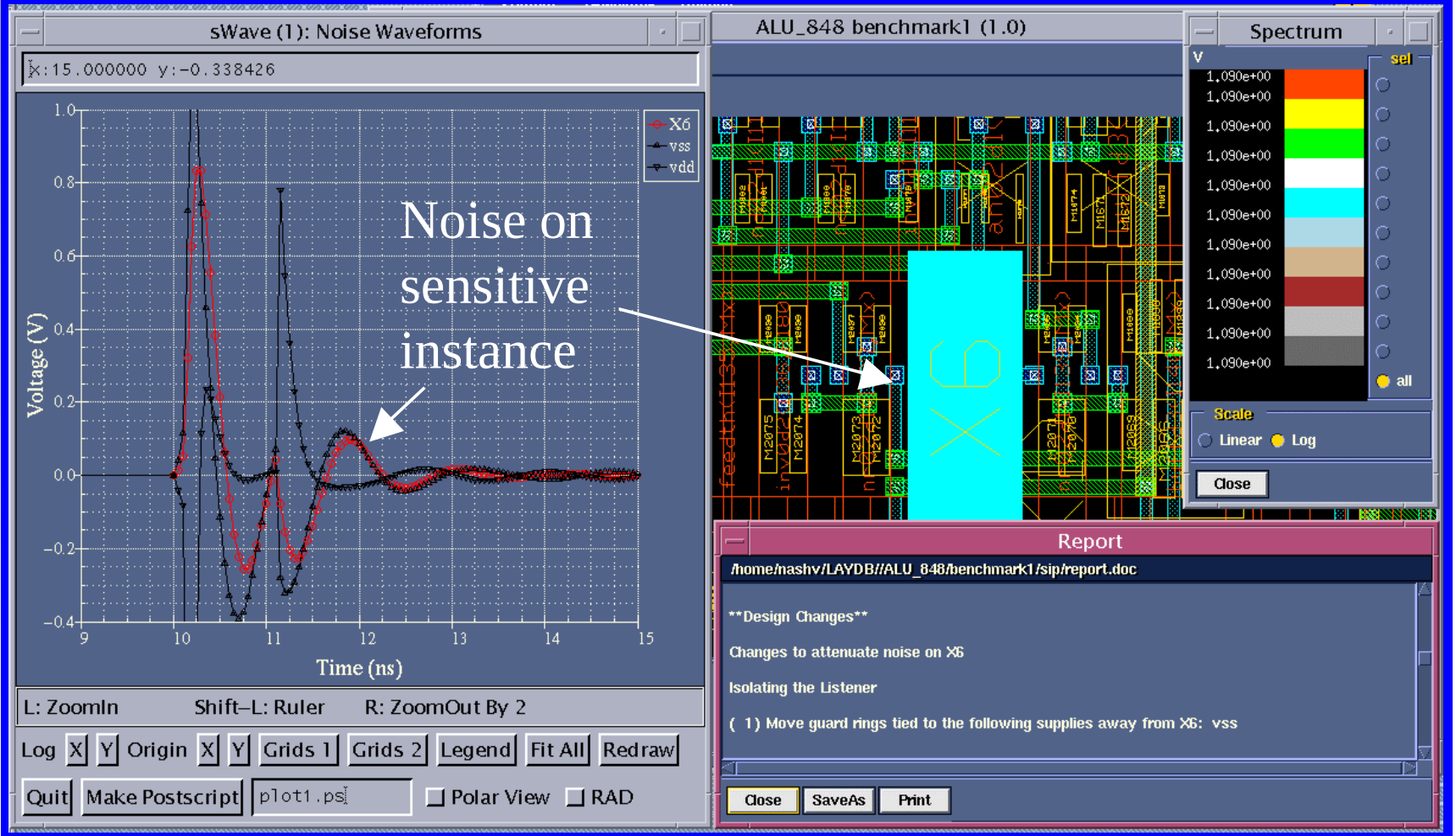
SeismIC - Input Requirements

- GDSII layout
- LVS/LPE output data for extraction of geometry information such as wells and substrate contacts
  - Beta version will support Dracula only
  - Plan is to add Calibre, Hercules and Clover interfaces
- SPICE netlist for extraction of connectivity
  - Output from LVS/LPE

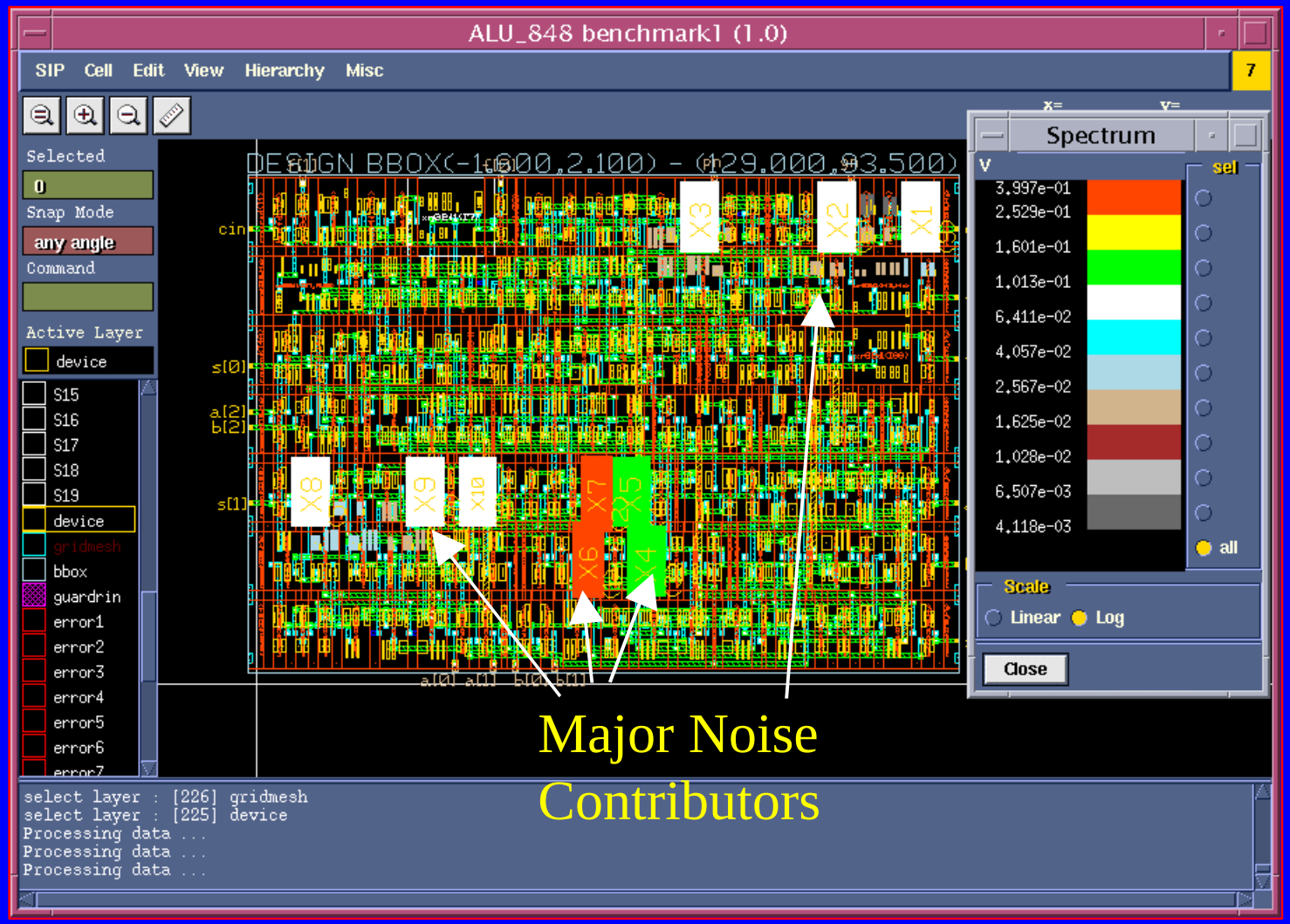
SeismIC - Input Requirements

- Switching activity from transistor-level simulation
  - Beta version will support HSPICE, PowerMill and StarSim
  - Plan is to add Star-MS, Mach-TA, ATTSIM
  - If not supplied, worst case switching is assumed
- Process technology file
  - substrate and well resistivity, thickness, etc.
- Package model (optional)
  - bond-wire / package pin inductance values, off-chip decoupling capacitance values etc.

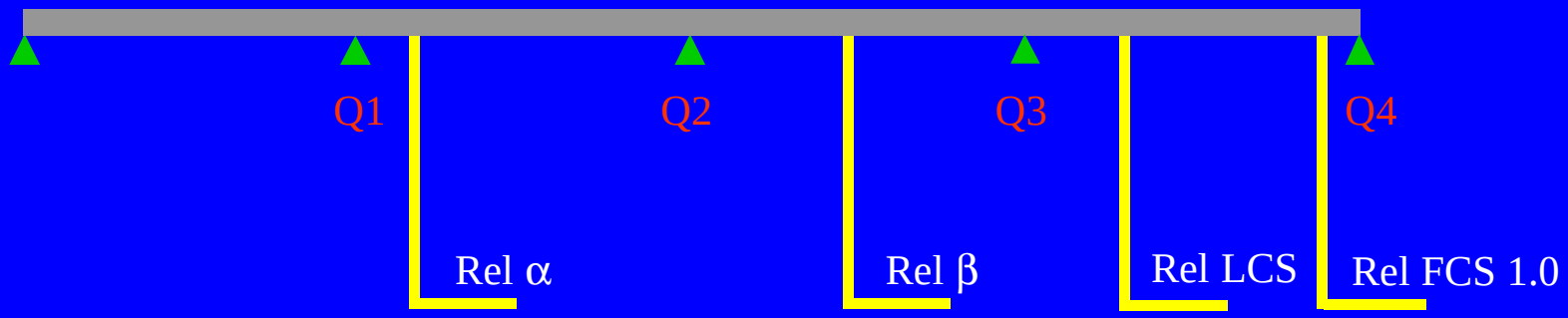
SeismIC Output



SeismIC Output



SeismIC Schedule



- Alpha release : May 1st 1999
- First beta release to early adopters : July 1999
- First limited customer ship release : Oct 1999
- Full customer ship release : Dec 1999

Summary

- Noise induced from high speed digital switching has become a significant problem in mixed signal design
- Noise coupling from supply, interconnects or devices via substrate can cause analog circuitry to fail
- SeismIC can identify the major sources of noise attacking sensitive analog transistors and advise how to improve their noise immunity
- SeismIC can help improve design quality, increase yield and shorten time to market