

datasheet

Cierto Virtual Component Co-Design (VCC) Environment

Answering the System Level Design Challenge

The Cierto[™] Virtual Component Co-Design (VCC) environment offers essential technology to manage the system-level design and integration crisis that threatens to undermine the delivery of electronics systems. The Cierto VCC environment, which is the result of the "Felix Initiative", has the following key benefits:

- Enables design productivity necessary to meet stringent time-to-market requirements
- Ensures a major increase in design flow predictability
- Integrates both system-level design and performance analysis to hardware and software implementation flows

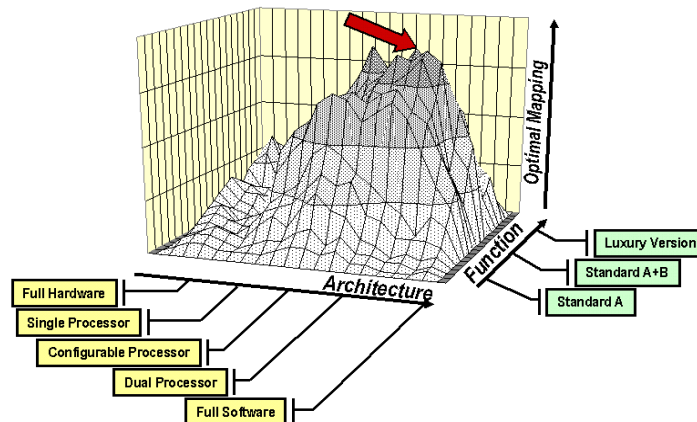
Typical applications for the Cierto VCC environment include wireless and wired communications, multimedia, and automotive. The traditional design methodology for embedded systems in these domains is comprised of a serial functional and architectural specification process, followed by hardware and software design with numerous iterations between each stage. Repairing defects in such a serial process has proven to be very costly.

The Cierto VCC environment, the industry's first system-level development environment for HW/SW co-design and IP reuse, seeks to overcome this traditional *ad hoc* design methodology. The Cierto VCC environment allows designers to confirm critical architectural decisions, such as the hardware and software partitioning of system functionality early in the design of both first-generation and derivative products.

Used as a technology for the configuration of SOC integration platforms, the Cierto VCC environment allows system companies and silicon vendors to optimize product specifications, shorten development cycles, and capitalize on the increased capabilities offered by multi-million gate integrated circuits. The Cierto VCC environment also provides software and hardware virtual component vendors with a "delivery vehicle" for promoting and distributing critical information to ensure successful "design-in" by their customers.

Enabling True HW/SW Co-Design

The Cierto VCC environment offers a comprehensive system-level design environment that allows the user to clearly differentiate between a behavior model, which identifies what the system does, and an architecture model, which identifies how the system is implemented. This clear differentiation between system function and architecture allows system designers to simulate the performance effects of a behavior running on a number of different architectures early in the design cycle.



A Complete Design Flow from System to Silicon

The Cierto VCC environment is part of a complete design flow and provides close integration with leading IP creation tools such as C, C++, MatLab, SDL and the Cadence Cierto™ signal processing worksystem (SPW).

The Cierto VCC environment's powerful links to implementation also bridge the gap between the system space and implementation-level integration and verification, using HW/SW co-verification (e.g., Affirma™ HW/SW verifier), HDL simulators (e.g., Affirma™ NC simulator) and software debuggers. For more information on the VCC links to implementation, please see the appropriate datasheet.

Target Users

The Cierto VCC environment uniquely addresses the needs of two types of users involved in today's embedded system design:

- **System designers** responsible for both system-on-chip and traditional system design. These designers evaluate, select, and integrate virtual components. The Cierto VCC environment lets these designers optimize product specifications, shorten development cycles, and capitalize on the increased capabilities offered by multimillion-gate integrated circuits.
- **Virtual component vendors** who provide software and hardware virtual components to system designers. The Cierto VCC environment gives these vendors a delivery vehicle for distributing both architecture models and critical simulation information to customers for use during system development.

Design Flow Predictability and Productivity

In the traditional serial electronic system design process, behavior and architecture specification are followed by hardware and software design. The opportunity to consider trade-offs in function and architecture performance occurs too late in the design flow for any changes to be made in either a timely or cost-effective manner. The Cierto VCC technology addresses this major problem.

With its sophisticated performance estimation and modeling techniques, the Cierto VCC environment offers system designers a methodology to make design tradeoffs at the system level by evaluating and comparing the impact of critical architecture choices. These critical choices revolve around (a) alternative hardware and software partitions, (b) bus and processor loading analysis, and (c) RTOS scheduling and resource contentions. Such tradeoffs can be analyzed effectively in Cierto VCC environment at a pre-implementation level, i.e., before hard commitments have to be made.

In addition to greatly increased predictability, system and implementation designers (in both the hardware and software domains) will experience dramatic productivity improvements when using the Cierto VCC environment. The hardware and software development flow can be brought together and pursued in parallel at the earliest point in the design process, i.e., right at the system level.

Cierto VCC Major Technology Components

The major Cierto VCC technology components are:

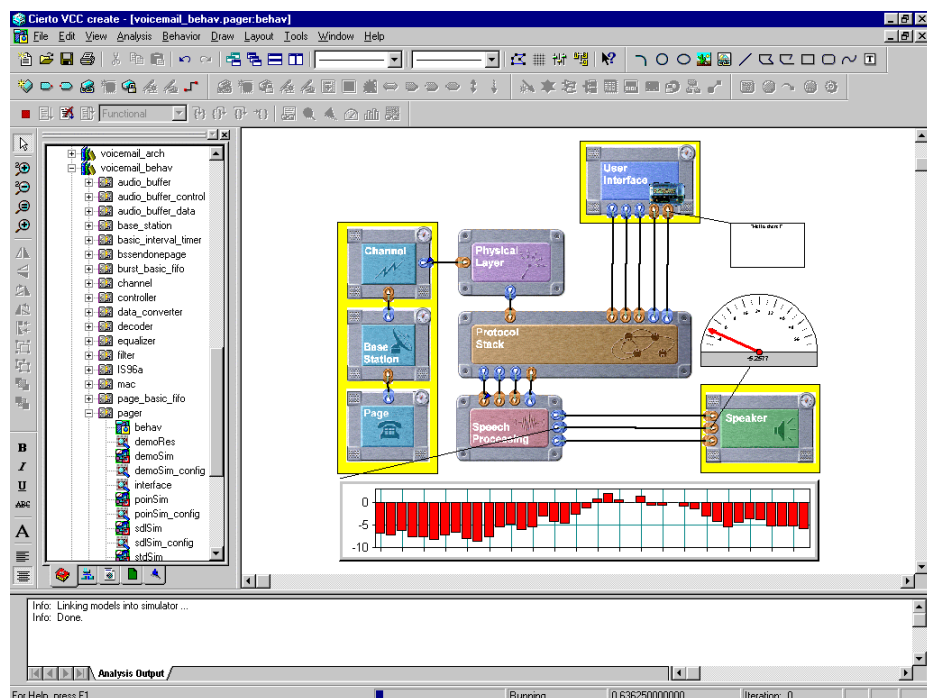
- **A behavior editor** that is used to capture an unambiguous executable behavior specification at a high level of abstraction using behavior models from vendor libraries, exported models from other design environments, or user-defined behavior models
- **A data type editor** which lets you either examine and edit defined abstract or implementation data types or create new ones
- **An architecture diagram editor** that captures a target architecture using high-level hardware and software architecture models and communication paths from vendor or user libraries
- **A mapping editor** that enables HW/SW and general architectural trade-off considerations by (a) associating each model in the behavior diagram with a hardware or software architecture element and (b) identifying its communication path as required
- **A simulator** that explores the design space by simulating the performance of each behavior as mapped onto an architectural element.
- **An analysis environment** in which selected trace output can be charted and graphed to evaluate the performance of the mapped design

- **Performance modeling techniques** that provide delay mechanisms that are used to simulate the execution of each behavior on the mapped architecture
- **Software estimation** that creates a performance model for C behavior that is mapped to software without actually running it either on a processor or an Instruction Set Simulator.
- **Communication refinement** that facilitates the refinement of abstract token level interface descriptions into the actual low level (signal level) interfaces
- **Links to implementation** that allow the user (a) to gradually refine a system toward implementation, (b) to explore communication alternatives, (c) to synthesize communication interfaces and (d) to generate the appropriate test and design data for downstream HW and SW implementation tools.

Building a Virtual Prototype of the System Functionality

The Cierto VCC environment is an environment in which the system designer works with graphical representations of virtual components, both functional and architectural. The Cierto VCC behavior diagram editor lets you capture the function of a system by creating a behavior diagram-- a collection of functional models that are wired together.

In top-down design flow using the Cierto VCC environment, designers create behavioral models by (a) placing an undefined block, (b) specifying the interface and the design parameters, and (c) generating a symbol for this block. Once the user specifies how this block is to be implemented, a window with a default template



for the model's behavior is generated. In bottom-up design flows using the Cierto VCC environment, designers use the hierarchical behavior diagram editor to instantiate graphical symbols representing already existing behavioral models, and then create the interconnections between these symbols.

Leverage Existing IP Investment

System designers have invested years developing functional and architectural IP models. There are also a number of best-in-class block authoring techniques that provide a flow from system level to RTL block implementation. In order to leverage the user's investment in IP and IP creation tools, the Cierto VCC tool environment allows designers to import functional system-level IP that have been generated using leading IP creation languages and technologies.

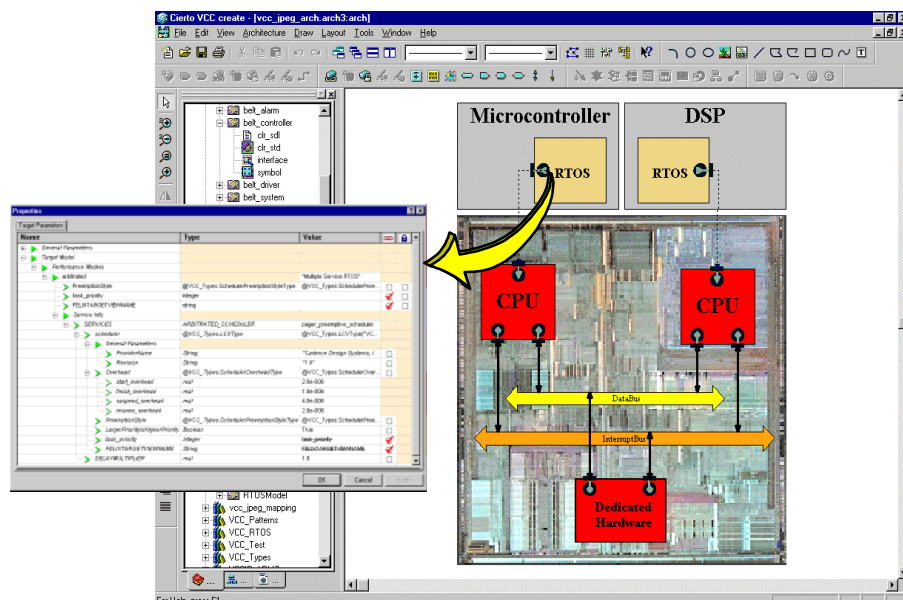
In particular, functional blocks can be imported from C, C++, SDL, MatLab, behavioral HDLs. Of course, the leading-edge libraries for wireless communications and multimedia applications from the Cadence Cierto signal processing worksystem may also be imported. Finally, the Cierto VCC discrete event simulation engine accepts models compliant to the OMI 4.0 standard.

Functional Simulation

This ability to import functional IP from a wide variety of sources into the Cierto VCC simulation environment allows designers to simulate the complete functionality of heterogeneous systems. This simulation then can be used as a golden executable functional specification.

Defining the Architectural Platform

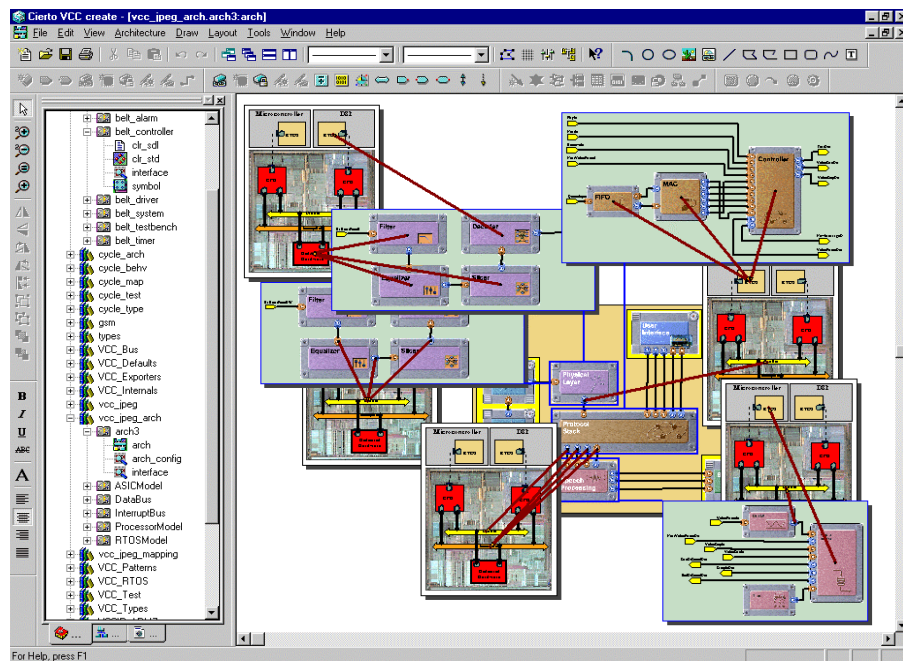
Using the VCC architecture diagram editor designers capture the abstract target architecture onto which the system function will be mapped. Since it is a complete co-design environment, the Cierto VCC environment supports essential architectural elements such



as CPUs, DSPs, RTOSs, buses, memories, and dedicated HW and SW. To allow fast design evaluation, these architectural elements are modeled at a higher level of abstraction than implementation-level C or HDL.

Mapping Function to Architecture

The Cierto VCC mapping diagram editor enables designers to map system functionality onto target architectural platforms. This mapping defines candidate hardware and software partitions and helps to identify the custom hardware needed to complete the system design. Designers also use the mapping diagram editor to refine communication wires.



Performance Simulation

Once a mapping diagram is completed, the system designers can evaluate the mapped design using performance simulation, which is enabled by software estimation and performance parameters that are annotated within timing free functional models.

Software Estimation

While interpretative processor simulation technology provides very accurate results for verification, its application for design evaluations is limited. On the other hand, the Cierto VCC environment enables painless estimation of software performance. In the Cierto VCC environment, microprocessors are modeled using a virtual machine instruction set, which is characterized in terms of instruction cycle delays. These delay calculations are used to profile the C code mapped to the processor, allowing fast performance tradeoff analysis.

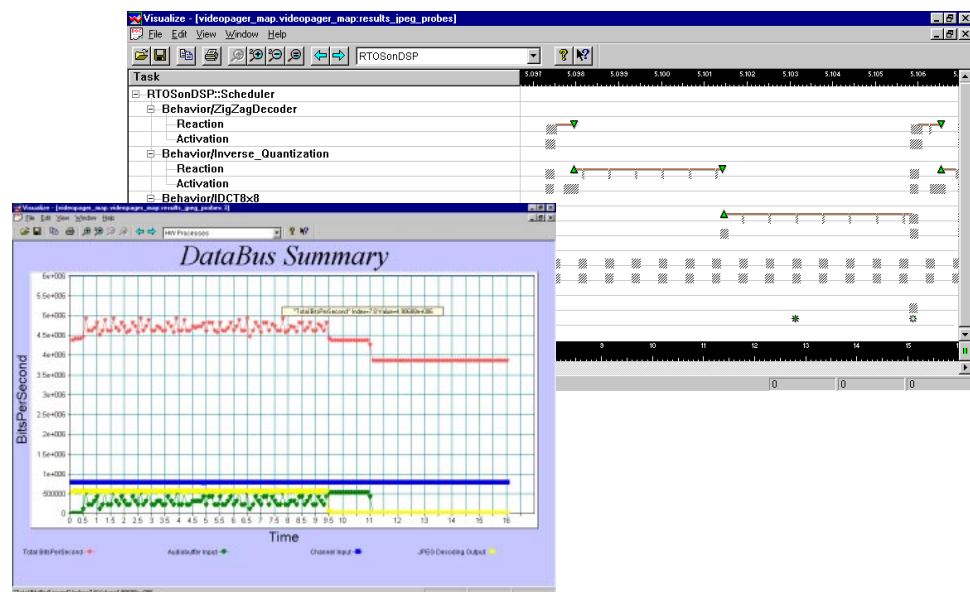
Performance Modeling

The Cierto VCC environment also offers a technique to annotate performance to timing free functions. This is used during the modeling of dedicated hardware or software. Different performance

Graphical Analysis Environment

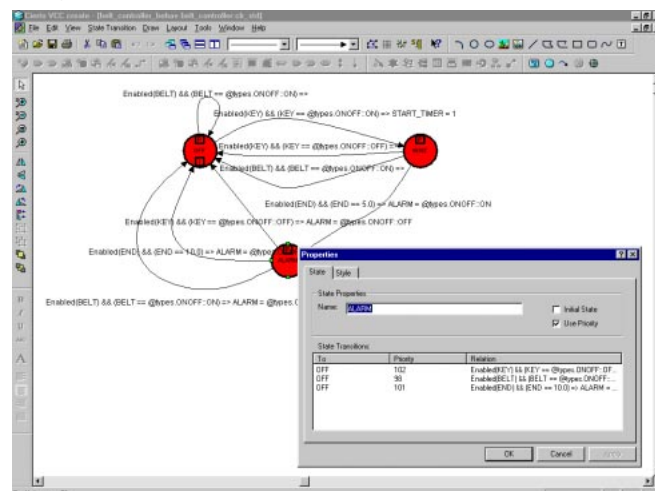
views can be used to represent implementations that have different execution speeds. The use of such performance modeling to evaluate the feasibility of potential hardware or software implementations allows much quicker analysis than would be allowed by either the slow execution of hardware using a HDL simulator or profiling of implementation-level software on an ISS.

The VCC environment offers comprehensive visualization techniques to display the results of functional and performance simulations. Users can easily customize two-dimensional, timeline, table and gantt charts to their particular analysis needs.



State Transition Diagram Technology

The Cierto VCC state transition diagram editor has two main applications. First, users can create control-dominated behavioral models and instantiate these model in the behavior diagram editor. Second, designers can create protocol converters to use in mapping diagrams.



Interface Refinement

The state transition diagram editor can also be used to capture additional behavior that represents the refined communication between two behavioral blocks. For example, suppose the communication between two blocks goes across a bus-- perhaps one behavior instance is mapped to hardware and one behavior instance is mapped to software. In this case, designers can create a state transition diagram that implements the interface to the bus. Later in the design process this state transition diagram can be attached to systems in the mapping diagram editor.

Data Type Editor

The data types editor lets users examine and edit defined data types or create new ones. The Cierto VCC environment supports several data types:

- **Object**, the base for all data types
- **Composite**, user-defined data structures, similar to C structures
- **Union**, user-defined data structures, similar to a union in C
- **Set**, user-defined enumerations, such as on/off, yes/no
- **Alias**, library elements that are aliased to something else
- **Integer and Real**, used to represent 32-bit integers and real data types (64-bit floating point). Integer and Real types allow sub-ranges, which must follow syntax rules similar to those used for mathematical ranges
- **Unsigned**, used to represent unsigned 32-bit integers
- **Boolean**, used to represent true/false values

Libraries

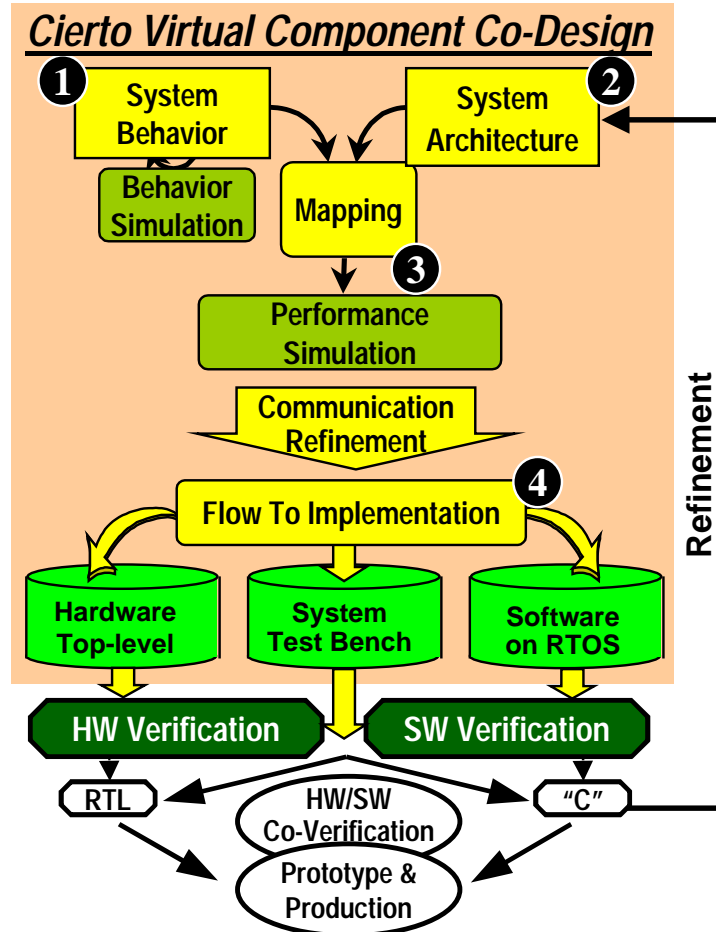
To increase productivity Cierto VCC comes with an extensive set of virtual component libraries. For effective testbenches the user can choose from a rich set of blocks representing arithmetic, counter, conversion, data structure access, delay, execution control, traffic generator and vector access functions. For busses and real time operating systems Cierto VCC provides a variety of standard bus arbitration and operating system scheduler schemes.

Services Eliminate Risk

The Cadence Methodology Services team offers service packages targeted at assisting Cierto VCC users to accelerate their learning curve and providing the right service at the right time to allow for productivity evolution. The basic core service include *Tool Training*, *Quickstart* and *Methodology Consulting*.

In order to efficiently model virtual components Cadence offers *IP Modeling Service* packages to IP providers for micro-controllers, digital signal processors, real time operating systems, busses, memories and dedicated hardware and software implementations.

A Complete Design Flow from System to Silicon



Cierto VCC Key Features

The Certo VCC environment offers the key technologies necessary to define the optimal combination of product function and architecture. When used to do derivative designs productivity is increased even further.

- Heterogeneous, *executable system specification*
- Definition, capture and configuration of *platform architecture*
- *Performance evaluation, HW/SW trade offs* prior to implementation
- Iteration through *different mapping scenarios*
- Gradual *refinement* of the design
- *Flows to rapid implementation*

For more information on Cadence's HW/SW Co-Design Solution please contact us at vcc_info@cadence.com or call your local Cadence sales representative.