CadMOS Design Technology, Inc.

Presents

Noise Analysis for IC Design

CadMOS
DESIGN WITH INTEGRITY

Company Introduction

- Privately held, founded in San Jose CA, Aug 1997
- 3 co-founders:
  - **Dr. Charlie Huang CEO**, Ex VP of R&D Synopsys/EPIC, originator of PowerMill, manager of PathMill
  - **Dr. Ken Shepard CTO**, Ex IBM Yorktown, G4 µP design lead, noise analysis expert
  - **Dr. Vinod Narayanan VP of R&D** , Ex IBM Yorktown, static noise analysis developer, static analysis expert
- $3m investment from venture capital (USVP) and other investors

Company Mission

Provide premium solutions to noise, signal integrity, and other electrical problems in advanced leading edge designs

Company Status

- Current staff of 18 people (9 R&D)
- Production release of PacifIC, Dec 98
  - Static noise analyzer for digital ICs
  - First orders received in Q1 1999 from TI and AMD
- Acquired technology and R&D staff of Apres Technologies, Inc. in January 1999
  - Pioneers in mixed signal substrate noise analysis
  - New product SeismIC, alpha released May 1st 1999

Customer Feedback

"We are incorporating PacifIC into our design flow to add an extra level of robustness and reliability to our designs, by ensuring that we have caught and corrected before tape out any potential noise problems."

Don Draper

AMD Fellow and K6-2 Circuit Design Manager

Customer Feedback

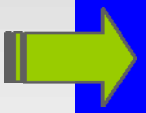
"We purchased PacifIC because we believe it can help us manage the noise immunity of our high performance DSP designs more effectively."

Robin C. Sarma

ASP-EDA, Texas Instruments Inc.

Technology Trends

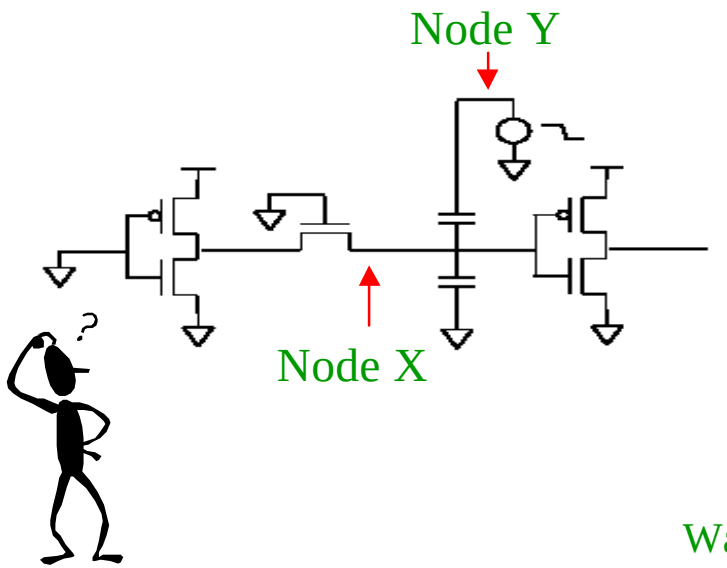
- Higher interconnect densities
- Faster clock frequencies
- Scaling of threshold voltages

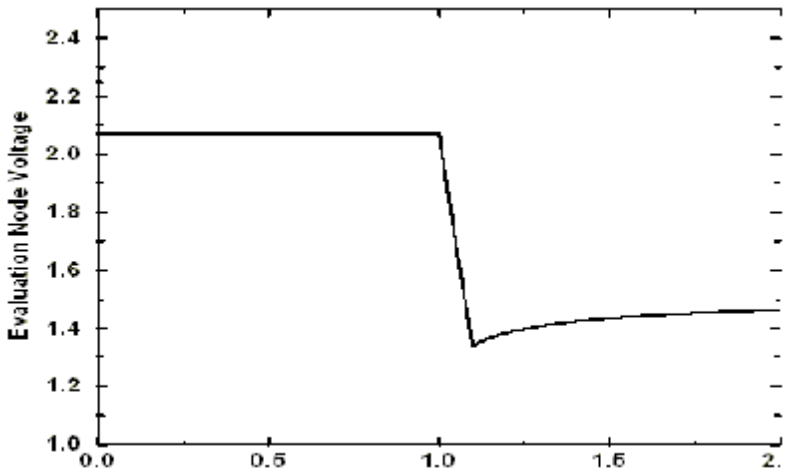


Dramatic increase of on-chip noise and decrease in noise immunity

What is Noise?

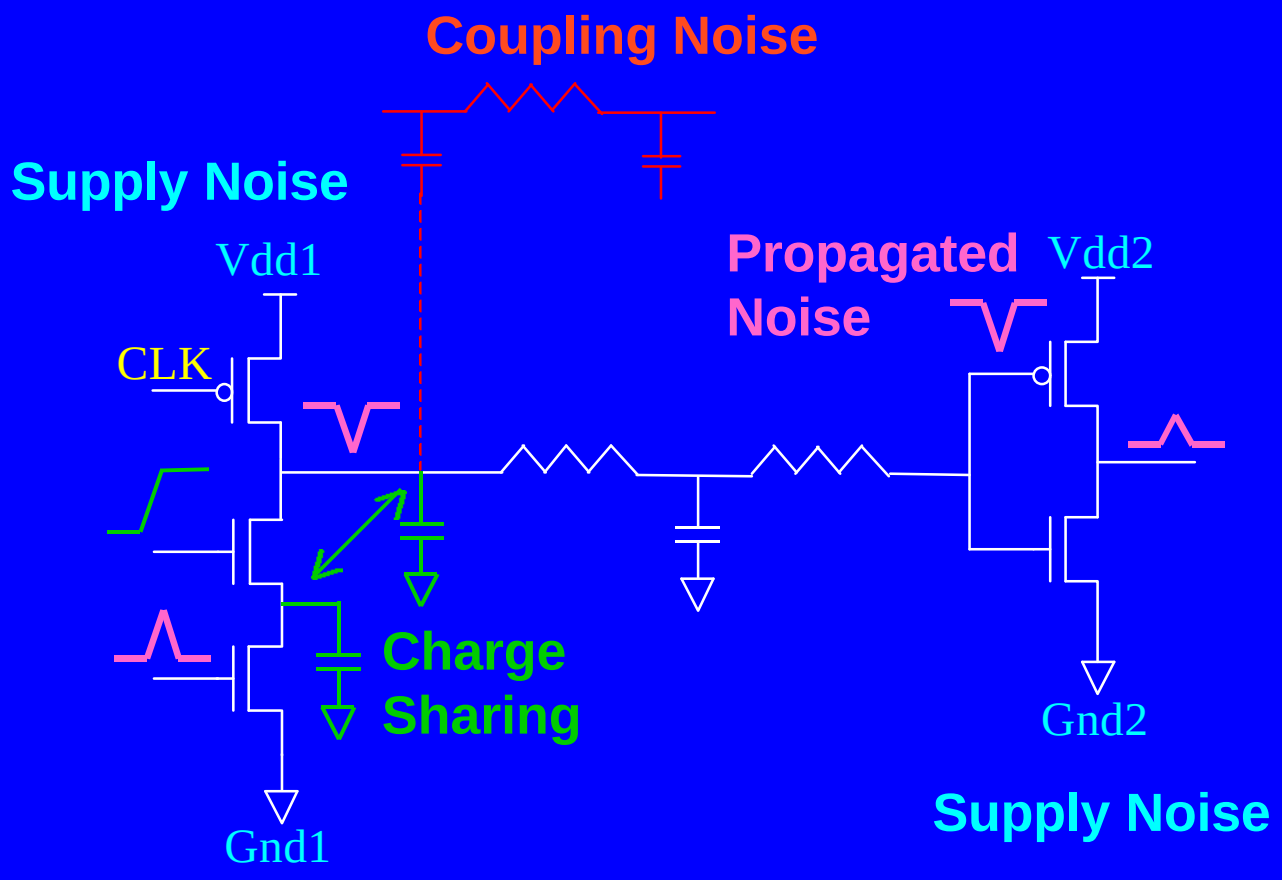
- Noise is any deviation in voltage in a circuit from nominal supply or ground
  - Noise can cause timing problems, functional failures and low yield
  - Noise problems are very difficult to debug





Waveform on Node X due to switching on node Y

Digital Noise Sources:



CadMOS Design Technology, Inc.

Introduces

PacifIC

Static Noise Analysis for Digital ICs

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PacifIC - Static Noise Analyzer

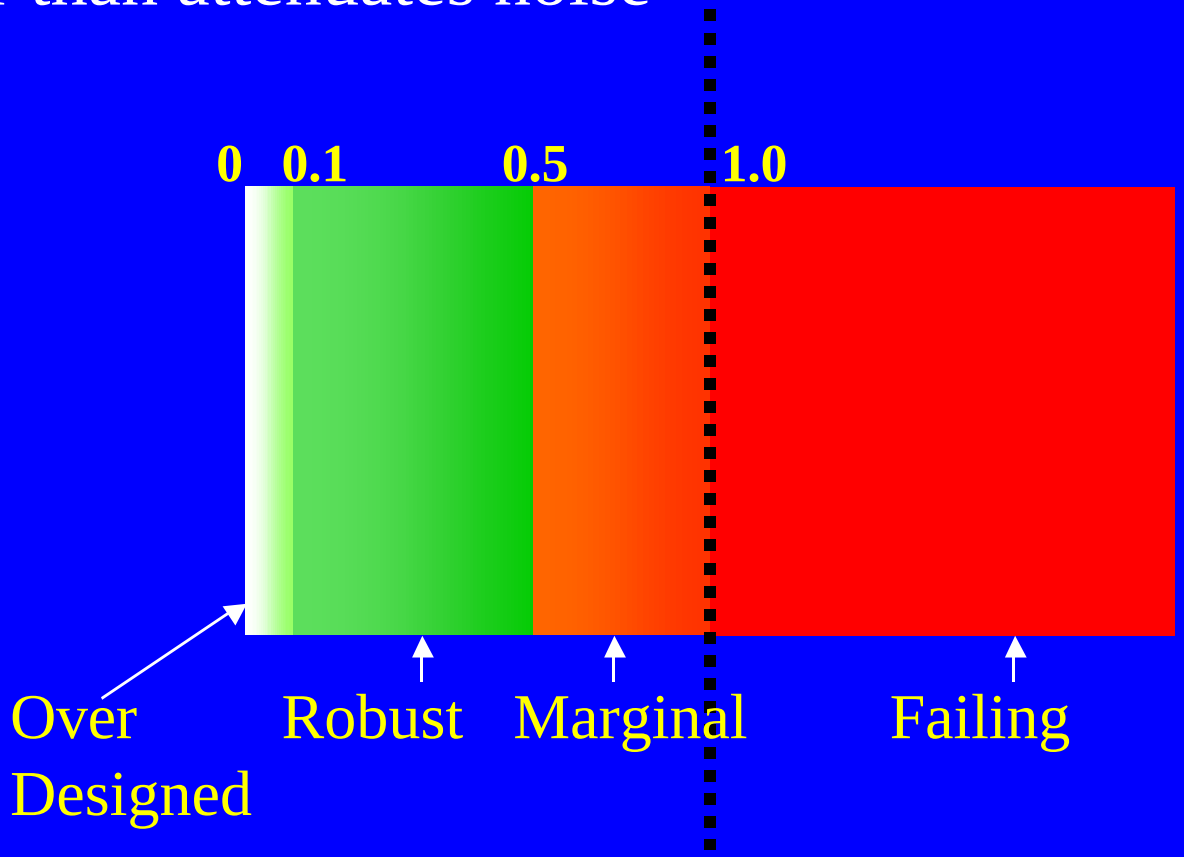
- Rigorously checks every node in the design without input vectors or design rules
  - Checks are based on the transient characteristics of noise
- Identifies nodes that are noise sensitive
- Identifies over design
  - Insensitive nodes may be over constrained by over sized feedback or pull-up devices

Benefits of Using PacifIC

- Fewer costly silicon re-spins needed to fix functional failures caused by noise.
- Improved yield by improving a design's noise immunity
- Improved performance or lower power by permitting more aggressive yet robust circuit design styles
- Reduced chip area through identifying unnecessary over design

Noise Sensitivity

- A node is deemed *sensitive* to noise if it amplifies rather than attenuates noise



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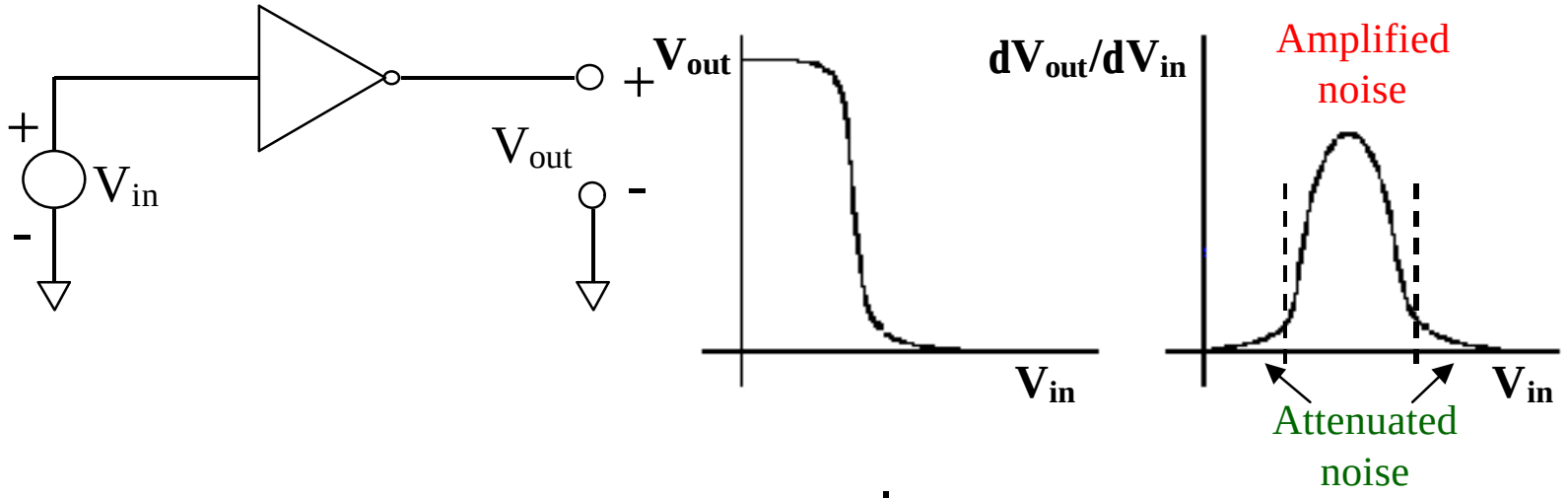
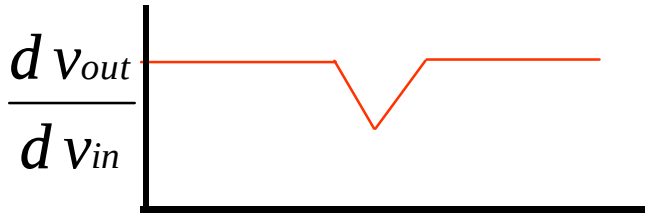
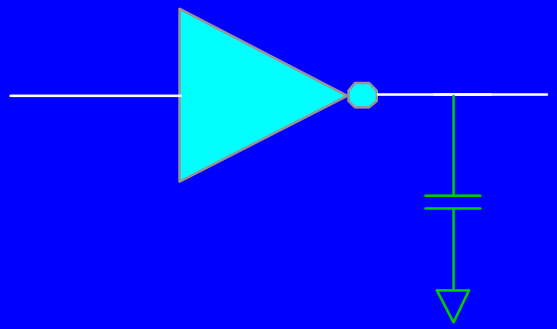
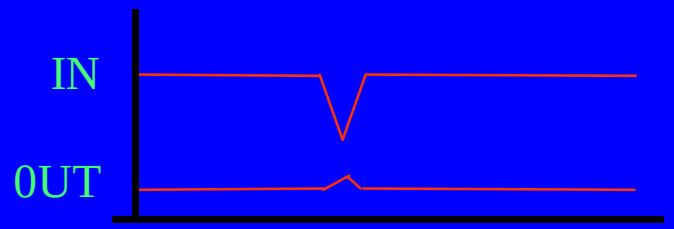


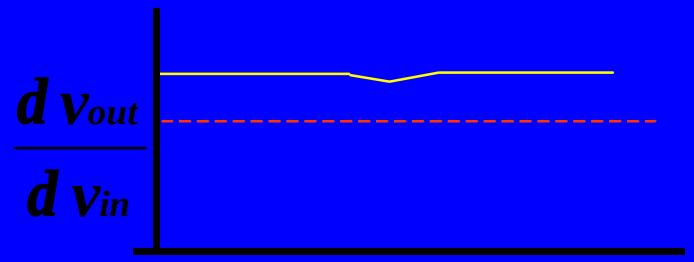
$$S(t) = \frac{d\,\mathrm{Vout}(t)}{d\,\mathrm{Vin}(t)} \leq 1$$



Transient Nature of Noise







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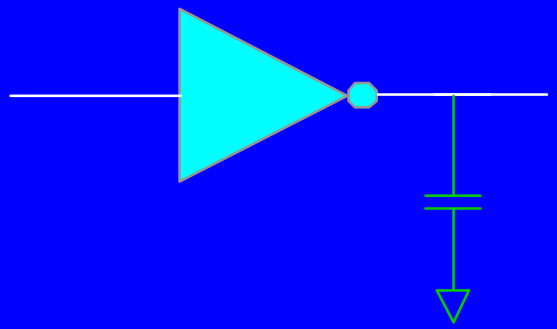
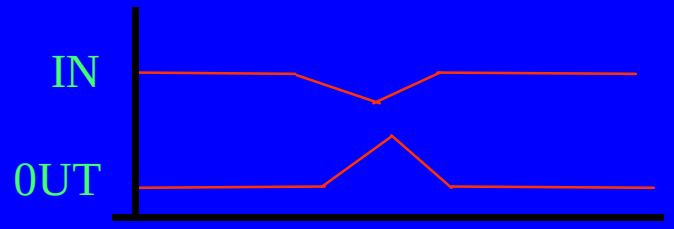
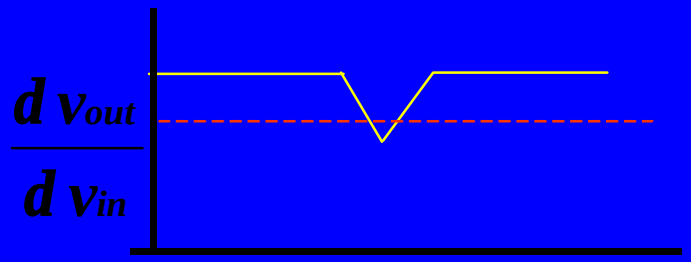
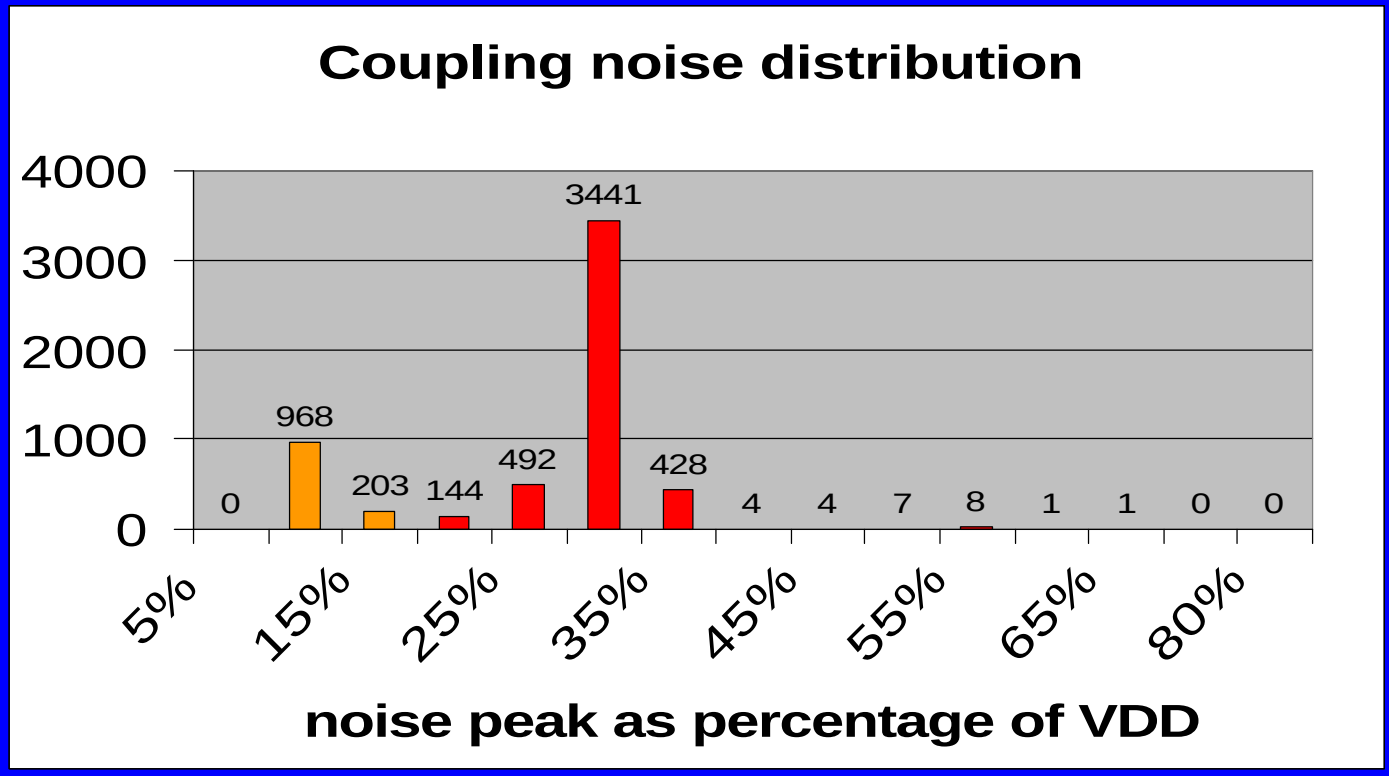




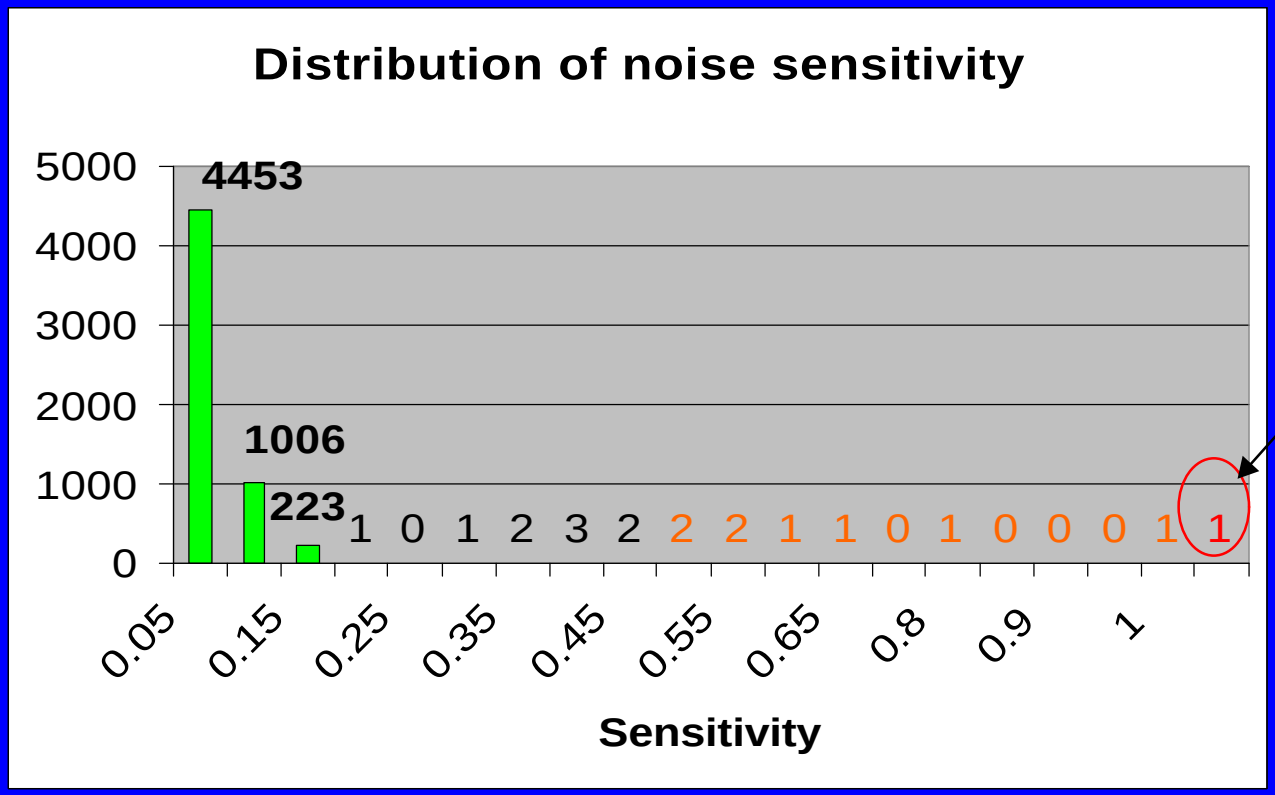


Noise Sensitivity Vs DC Margin



- Many nets (4.5K) have considerable noise > 25% VDD
- Implies examination of 4.5K potential problems

Noise Sensitivity Vs DC Margin



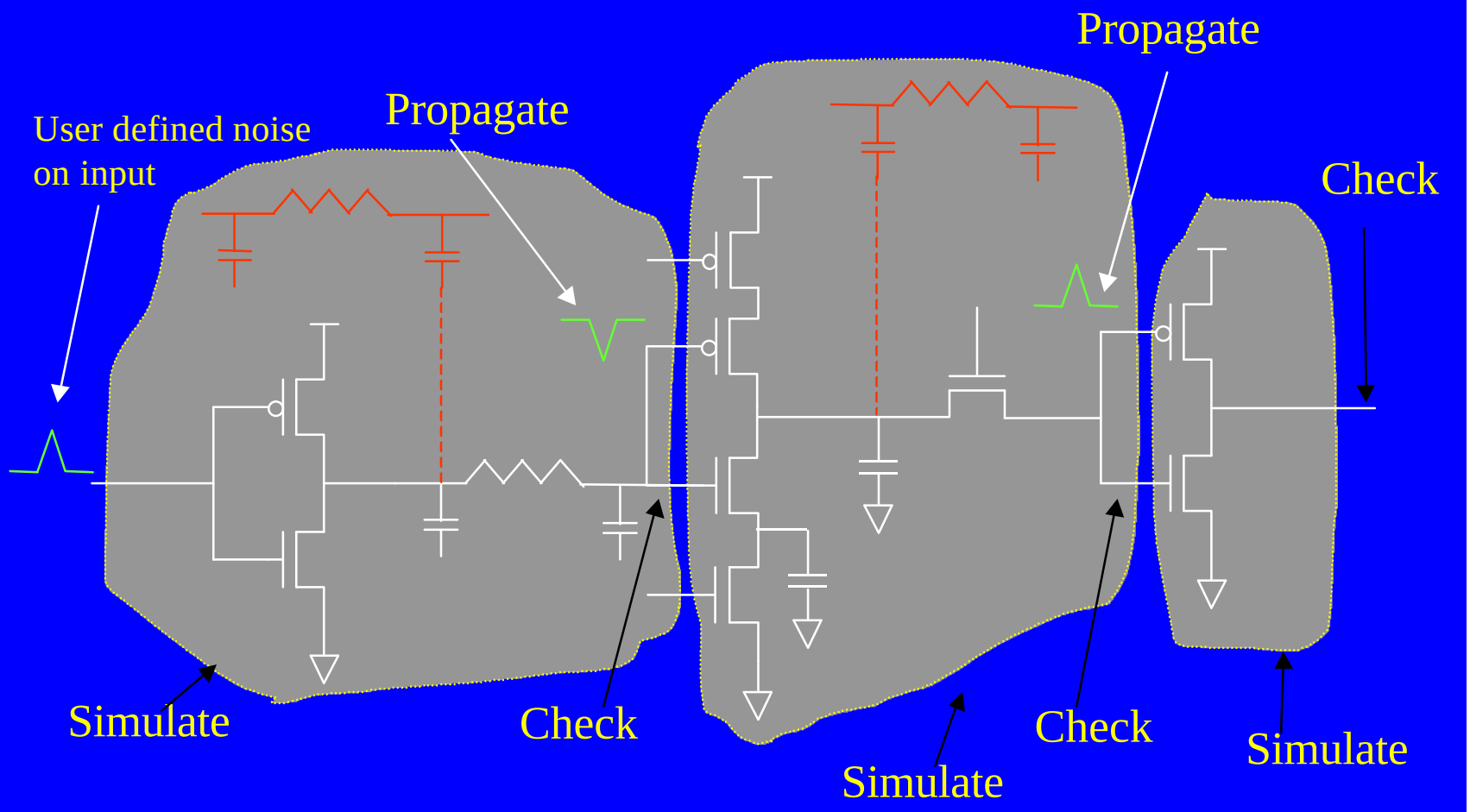
Failing Net

- Only 9 nets warrant investigation
- Implies 500X less work!

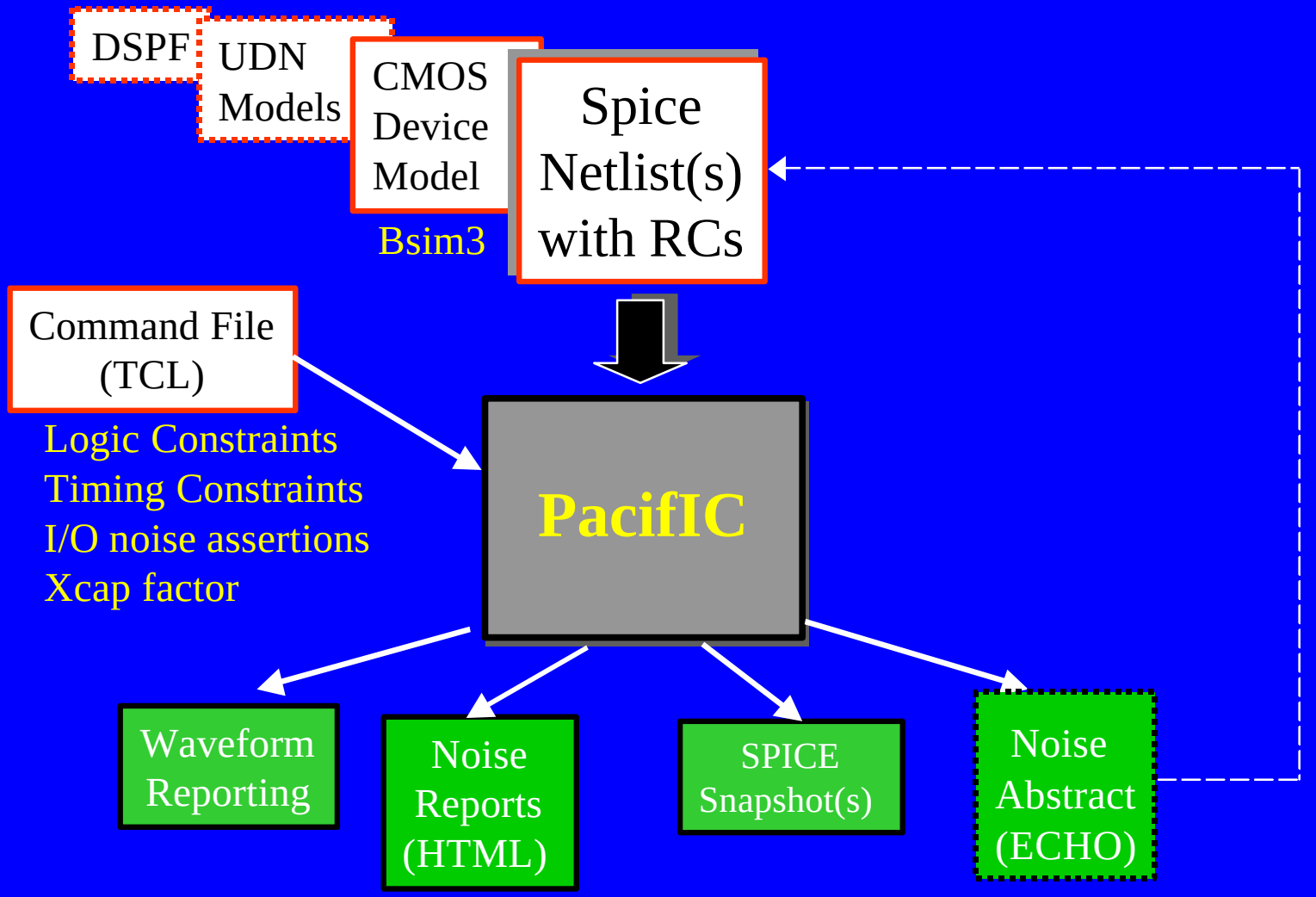
PacifIC - Core Technology

- Built-in transient analysis engine for localized simulation
- Sophisticated logic analysis to determine stimulus for worst case noise scenarios
- Built in noise sensitivity metric
  - Determines the transient sensitivity of receiving circuitry to noise
- Krylov based RLC interconnect modeling included as native in the simulator

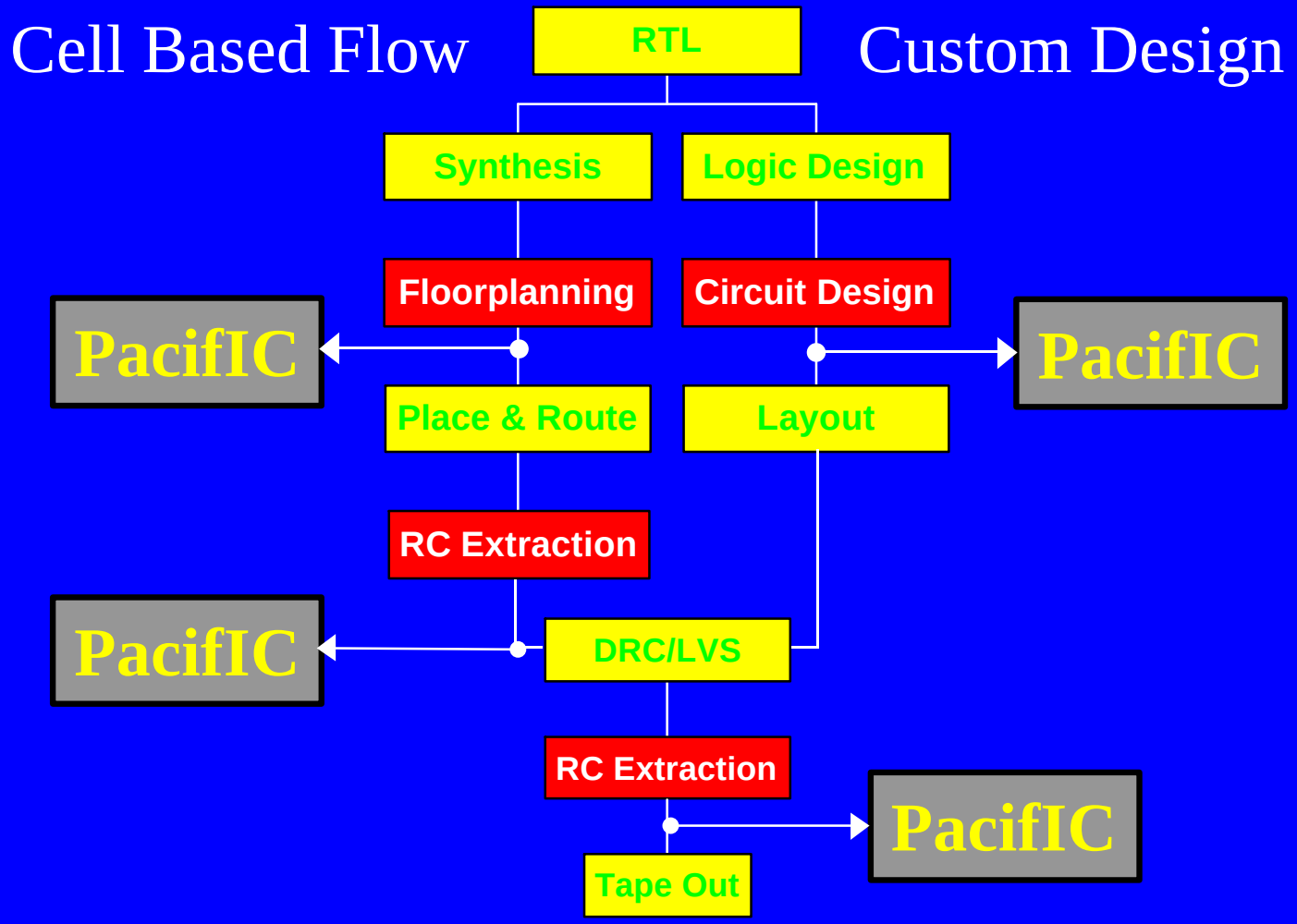
PacifIC : Static Noise Analysis



PacifIC : Data Flow



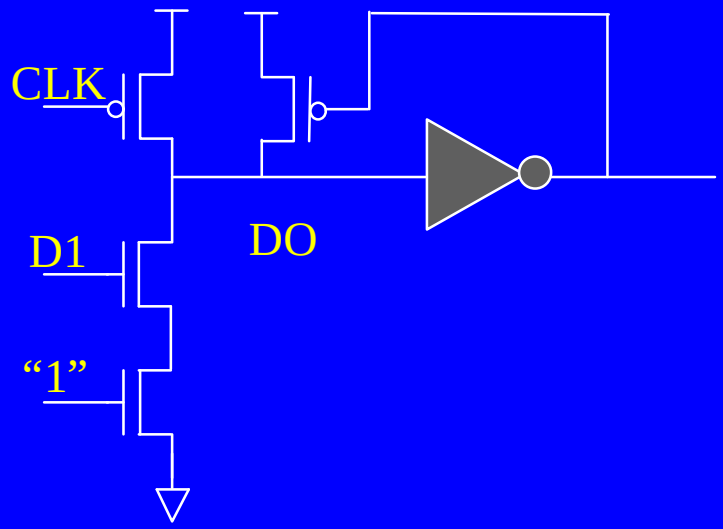
PacifIC in the Design Flow



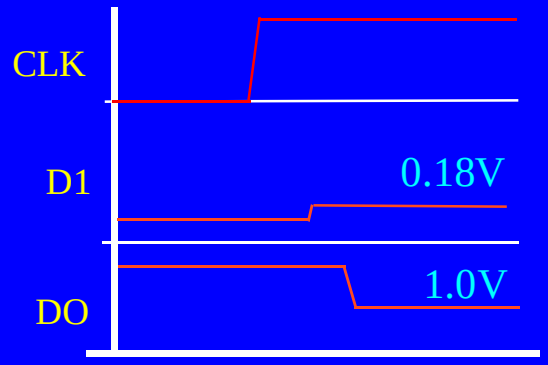
PacifIC : Features

- Propagates worst-case noise from primary inputs to primary outputs
  - Includes full PWL noise waveform propagation
- Analyzes the impact of supply and substrate noise
  - Supplied by the user as fixed variations
- Supports user defined constraints
  - logic : xor, and, or, not, mutex
  - timing : arrival time, slew
- Supports TCL commands based on pattern matching, wildcarding and sub-circuit type

Example - Leakage

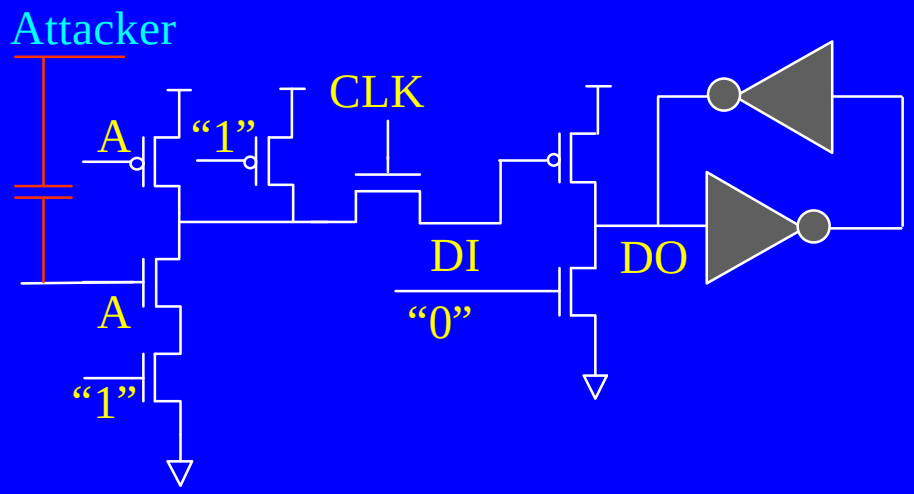


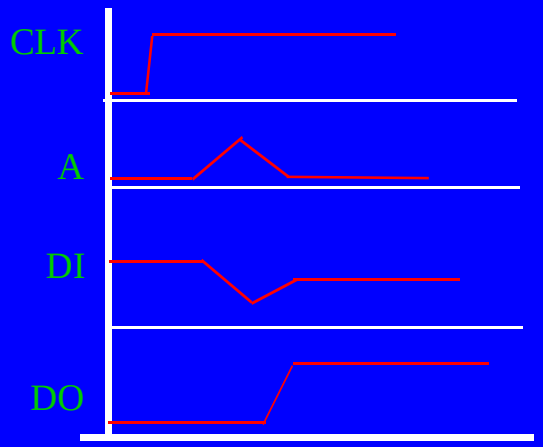
- 32-Bit Integer Adder
  - 0.25µ, 1.8V process
  - 36K transistors
  - 565 Xcaps, 172K Rs



Run Time	Memory	Failures
19m	104Mb	36

Example - Coupling

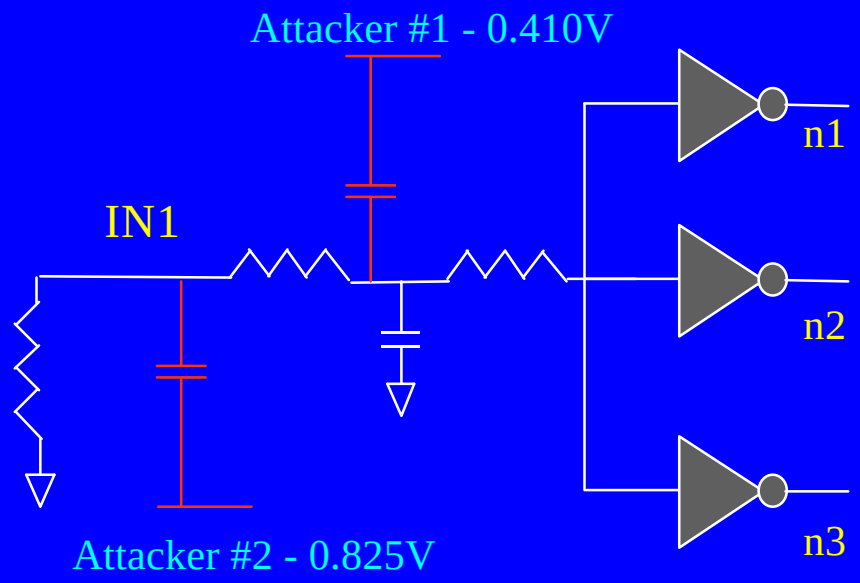


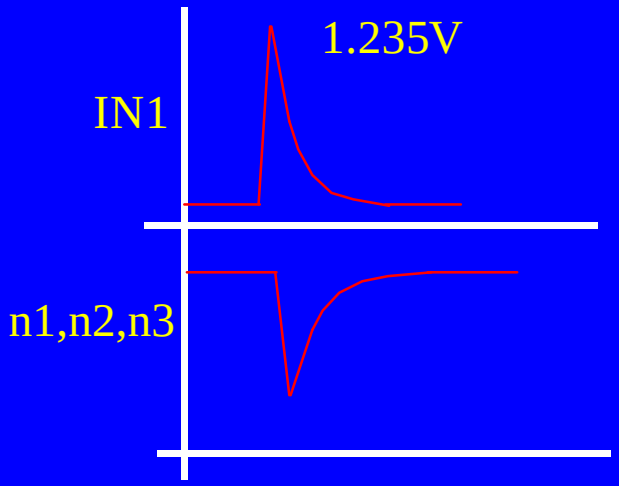


- **Microprocessor Cache**
  - 0.25µ, 1.8V process
  - 467K transistors
    - 54K flat transistor, 8 UDNs
  - 9K Xcaps, 345 Rs

Run Time	Memory	Failures
1h 4m	186Mb	46

Example - Coupling

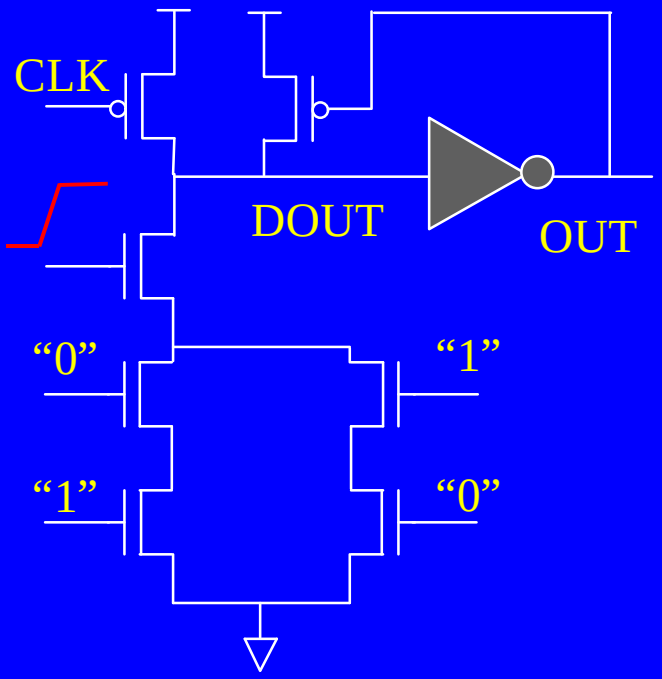


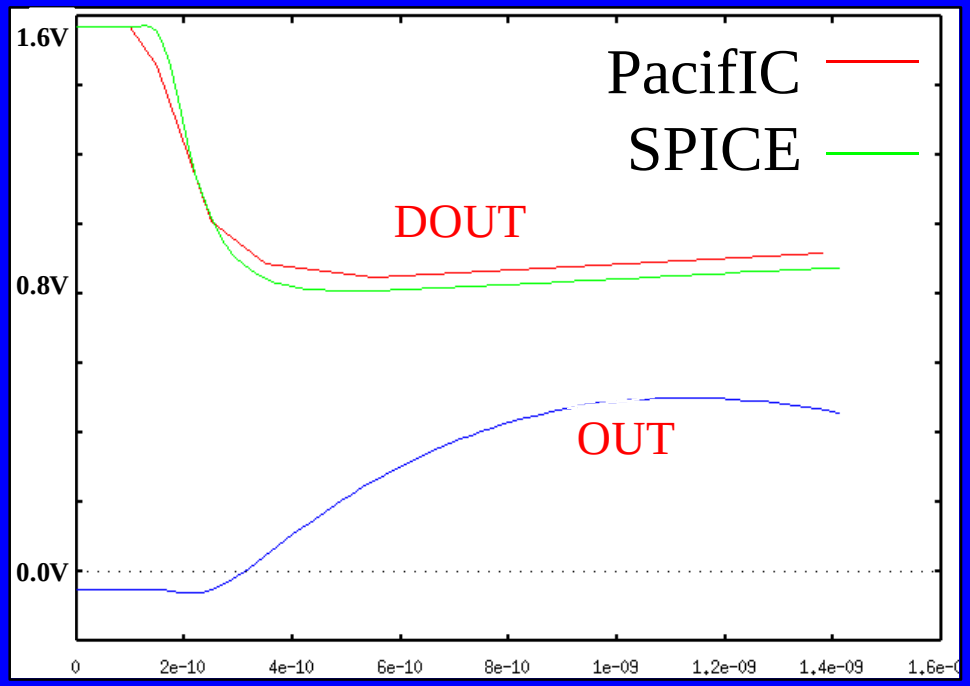


- Standard Cell Block
  - 0.25µ, 1.5V process
  - 98K transistors
  - 1.5M Rs, 2.8M Xcaps

Run Time	Memory	Failures
44m	420Mb	9

Example - Charge Sharing

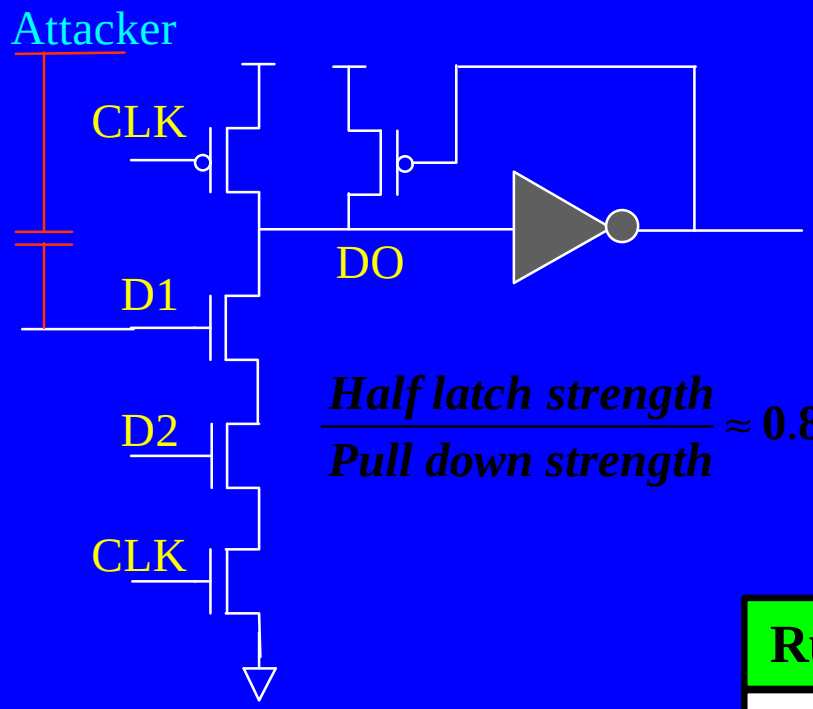




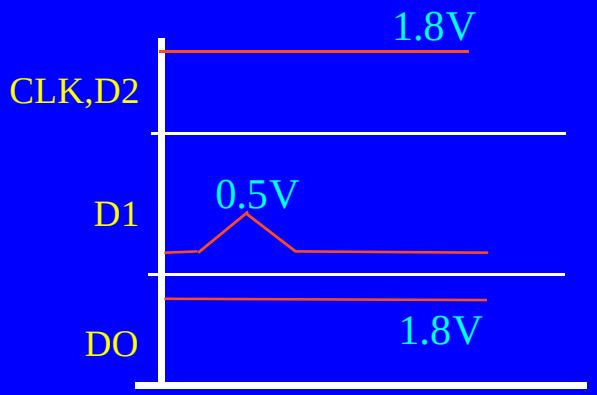
- Custom µP Block
  - 0.28µ, 1.6V process
  - 325K transistors
  - 153K Xcaps

Run Time	Memory	Failures
2h 9m	185Mb	484

Example - Over Design



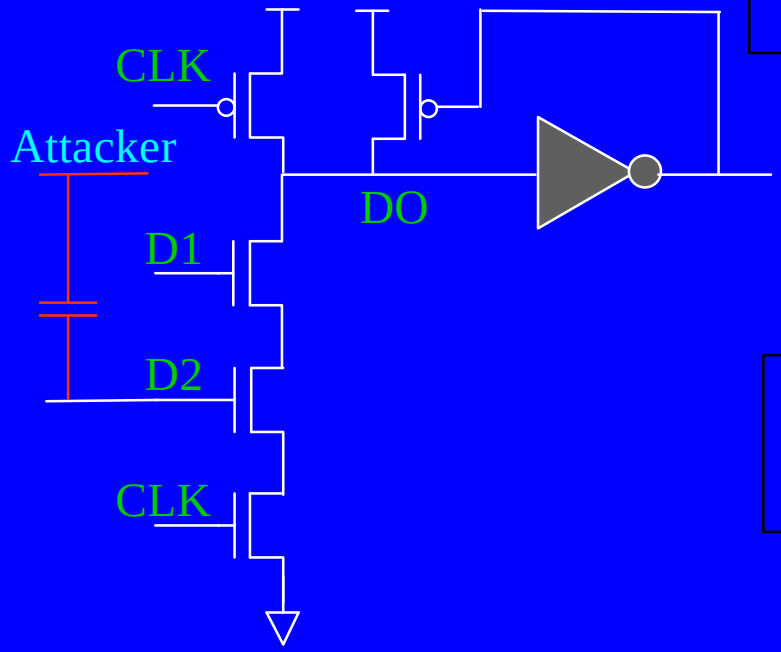
$$\frac{\textit{Half latch strength}}{\textit{Pull down strength}} \approx 0.8$$

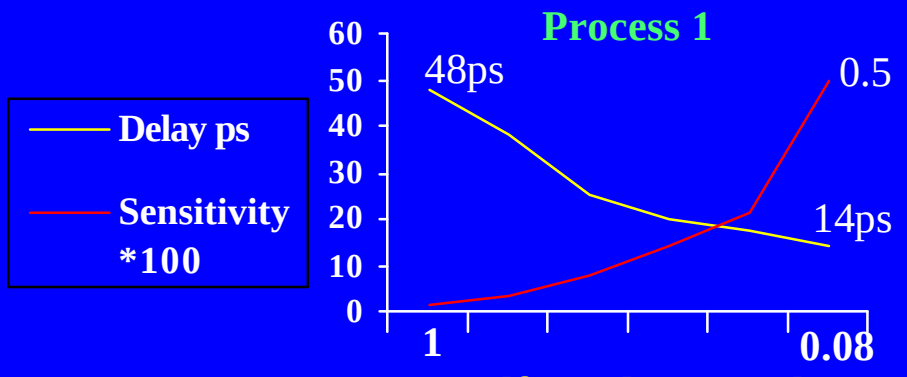


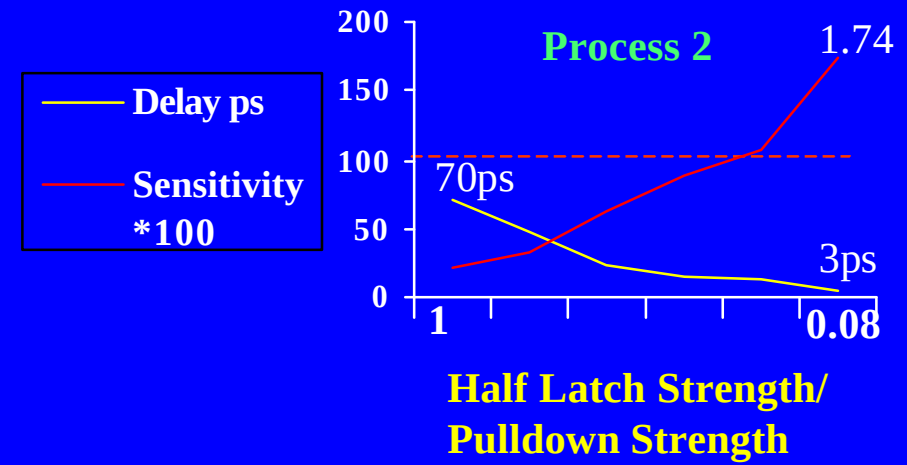
Run Time	Memory	Failures
6m	20Mb	0

- 64 bit adder
  - 0.18µ, 1.8V process
  - 9K transistors, 112K Xcaps, 48K Rs

Over Design cont.





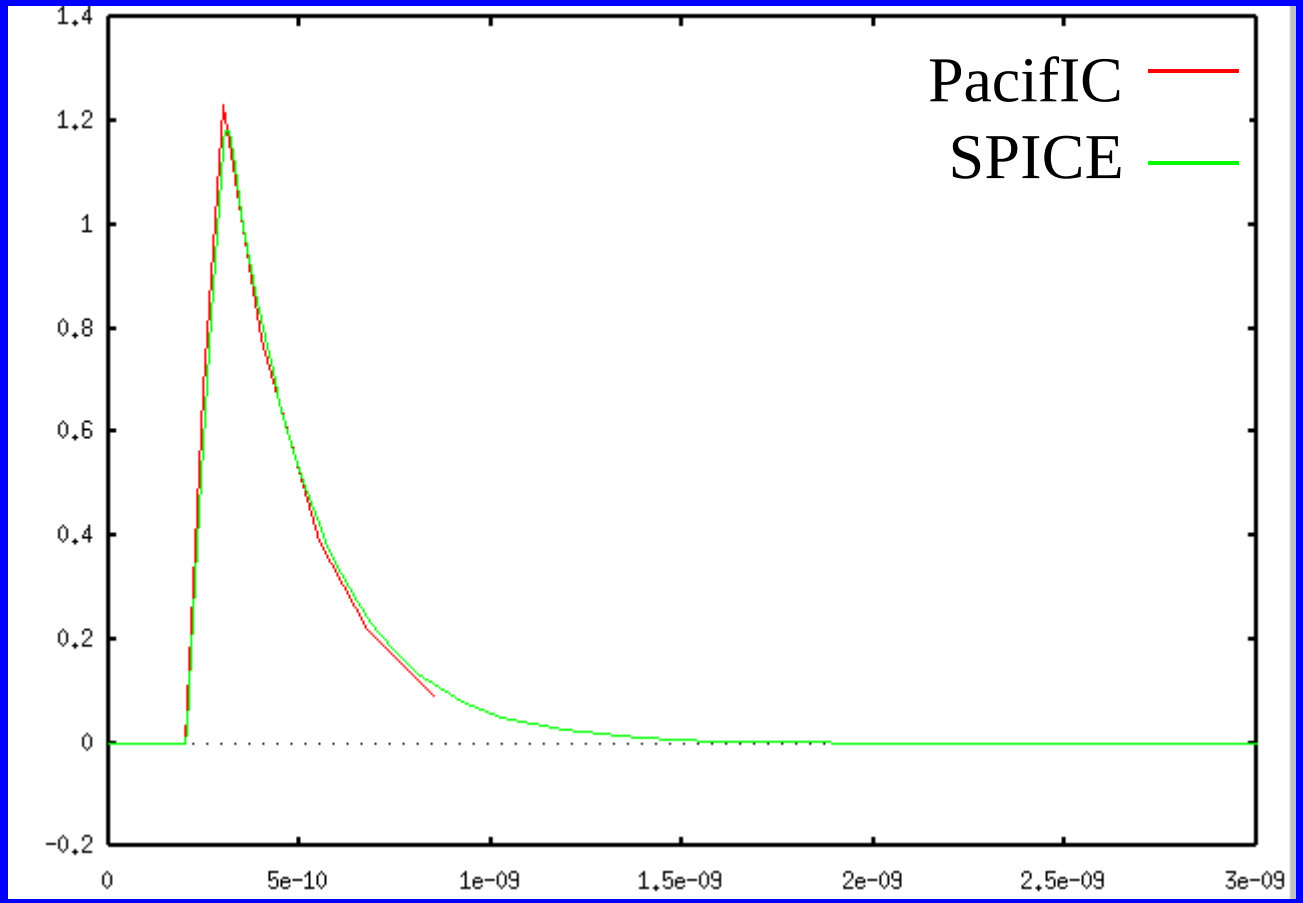


PacifIC Benchmark Summary

Xtrs	Rs	Xcaps	Runtime	Memory	Failures
17K	0	0	0:06:07	16MB	0(0)
47K	0	0	0:10:51	41MB	69(11)
37K	545K	1.6K	0:18:04	162MB	3(1)
95K	1.54M	2.8M	0:44:31	420MB	9(1)
54K	345	9.5K	1:04:44	185MB	46(6)
325K	0	153K	2:08:58	185MB	484(13)
653K	1.2M	2M	3:00:57	560MB	1(1)

- All benchmarks run on Sun UltraSPARC 60, time in hrs
- Failure numbers in parentheses are the number of unique failures

PacifIC Vs SPICE



Summary

- Noise has become a significant problem for UDSM
- Static noise analysis is key for large digital designs
- PacifIC can isolate nodes with low noise immunity
- PacifIC can help improve design quality, increase yield and shorten time to market