



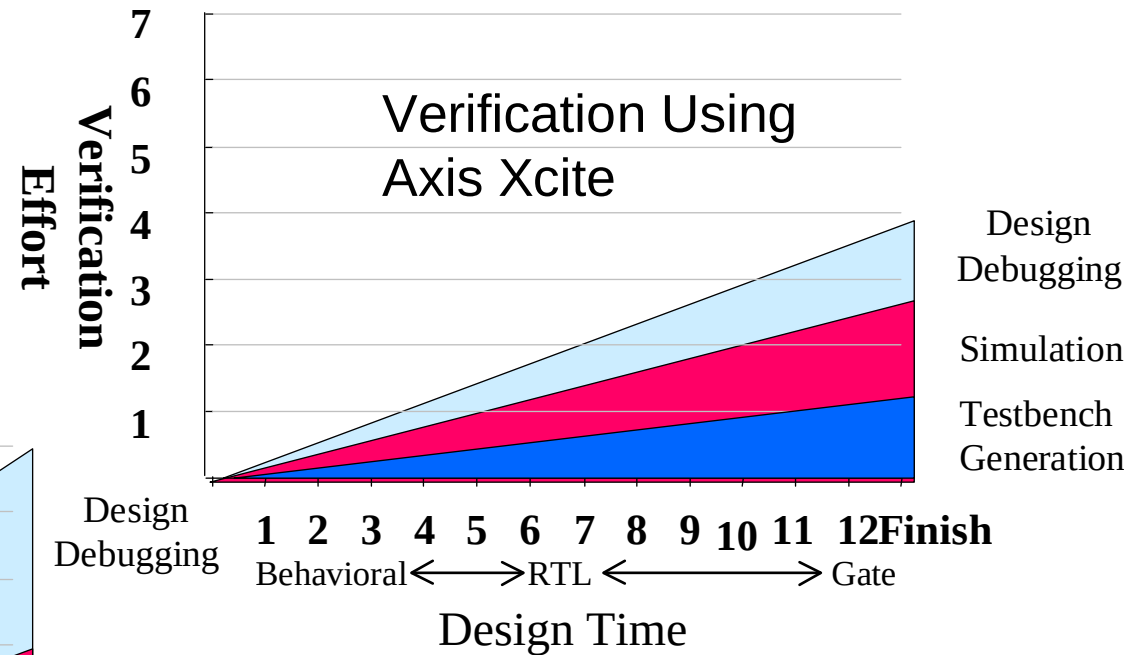
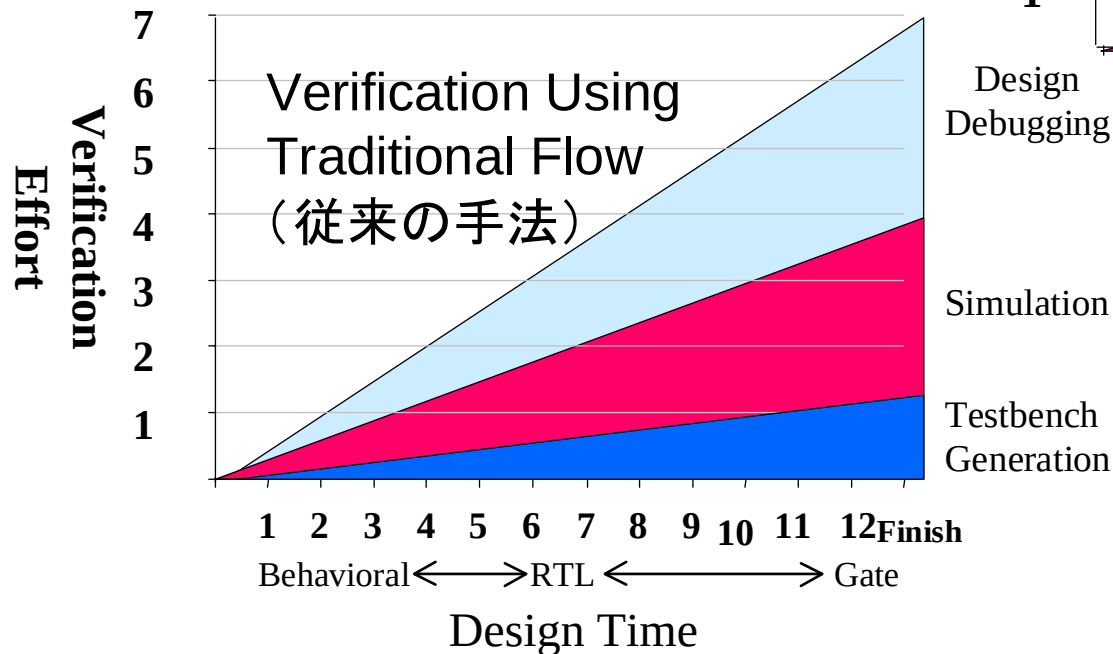
Axis Systems

Fast Move

Axis Systems Mission

- ◆ Axis Systems, Inc. is a technology leader in the logic design verification market. Founded in 1996, the company offers breakthrough technologies and high-speed simulation acceleration products to verify electronic systems and systems-on-a-chip designs.

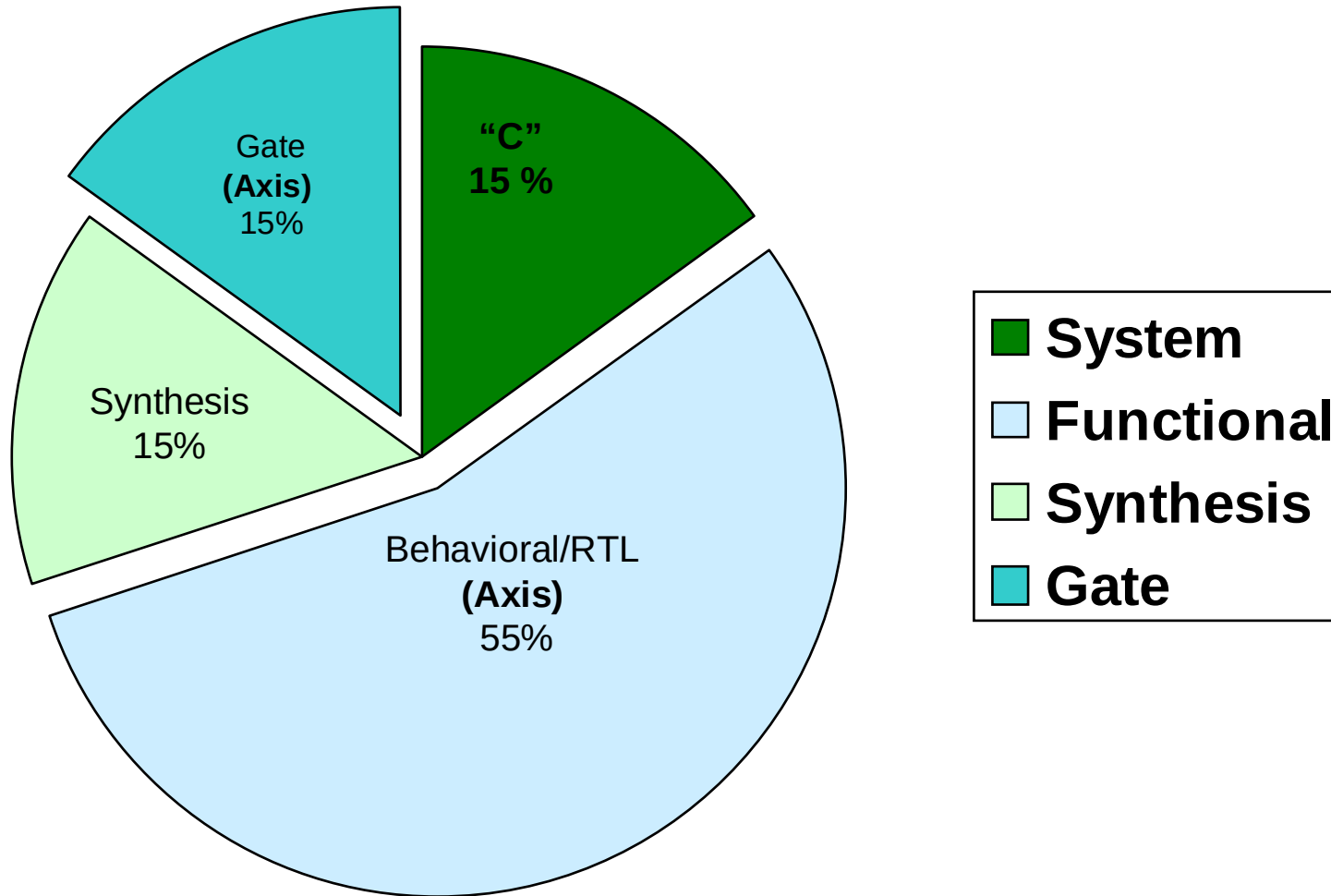
Verification Challenge



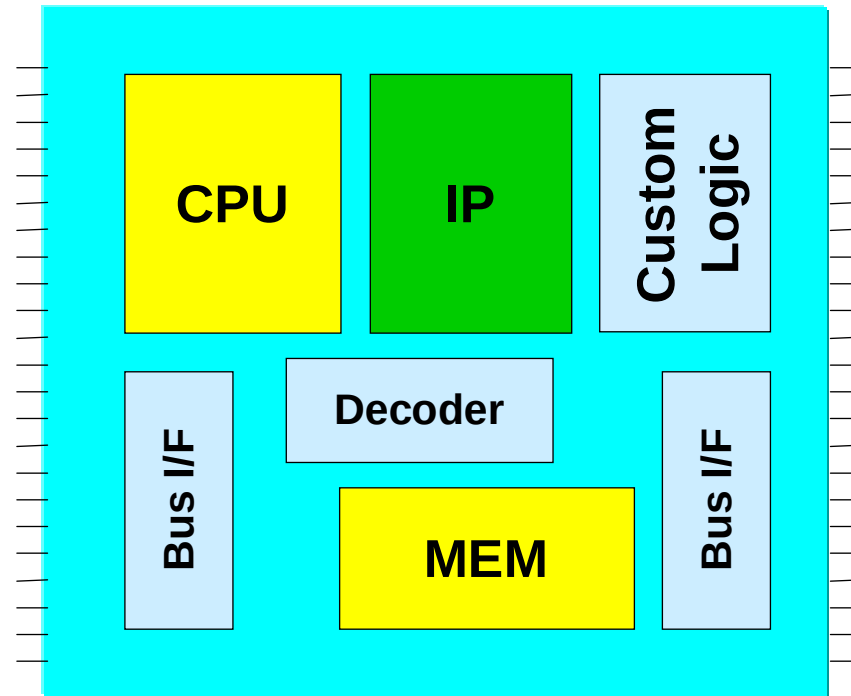
Reduce verification effort by half = faster time to market

検証作業の労力を半減
＝製品をより早く市場に

The Design Process



Simulation Spectrum



Behavioral	➡	Xcite Xsim
RTL	➡	Xcite Xsim & RCC
Gate	➡	Xcite Xsim & RCC

Axis System Verification Focus

- ◆ Offer **simulation acceleration** by orders of magnitude with new ReConfigurable Computing (RCC) technology (RCCによるシミュレーションの高速化)
- ◆ Preserve **user's current design methodology** with easy to use and easy to setup verification products = plug and play (既存の設計環境に適合し使いやすい)
- ◆ Provide **advanced debugging tools** to quickly pinpoint design problems and provide fast turn around time (独自のデバッグ機能によるTATの短縮)

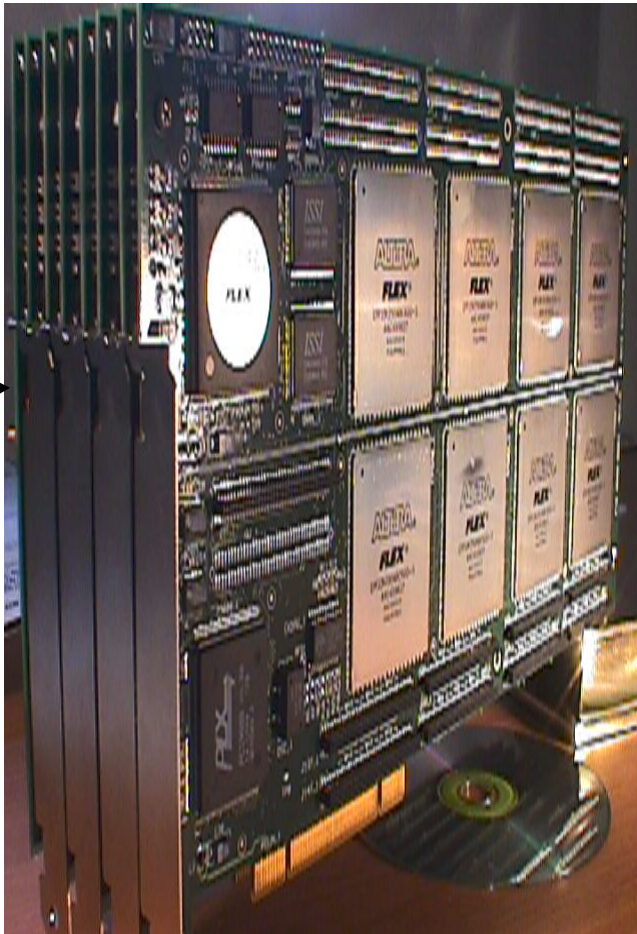
Xsim Overview

- ◆ Best Debugging Verilog Simulator
Performance + Flexibility
- ◆ Provide interactive features previously available only in interpreted simulators
- ◆ Native-code Verilog simulator running on Sun Microsystems workstation
- ◆ Complies with IEEE standards including PLI 1.0
- ◆ Easy migration path to RCC accelerated simulation
- ◆ Obtain functional closure with Xaminer functionality

Xcite-1000 RCC Co-Processor

4 million gate capacity
16M bits memory capacity

RCC PCI
Plug-in
Boards



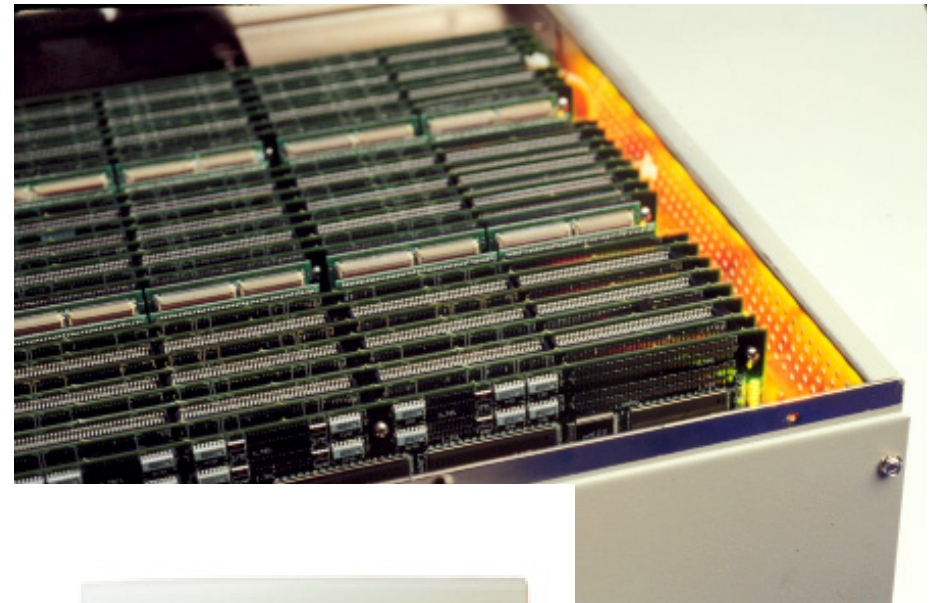
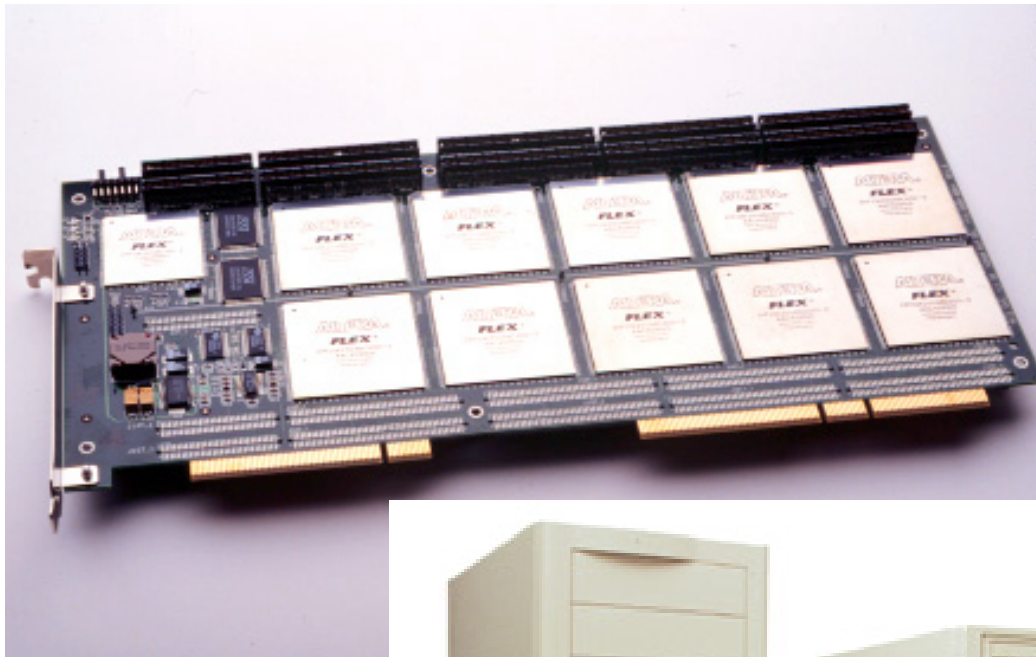
8 Board
Configuration
with Altera 10K Chips

Xcite Software:
-Xcite Simulator
-Xcite RCC Compiler



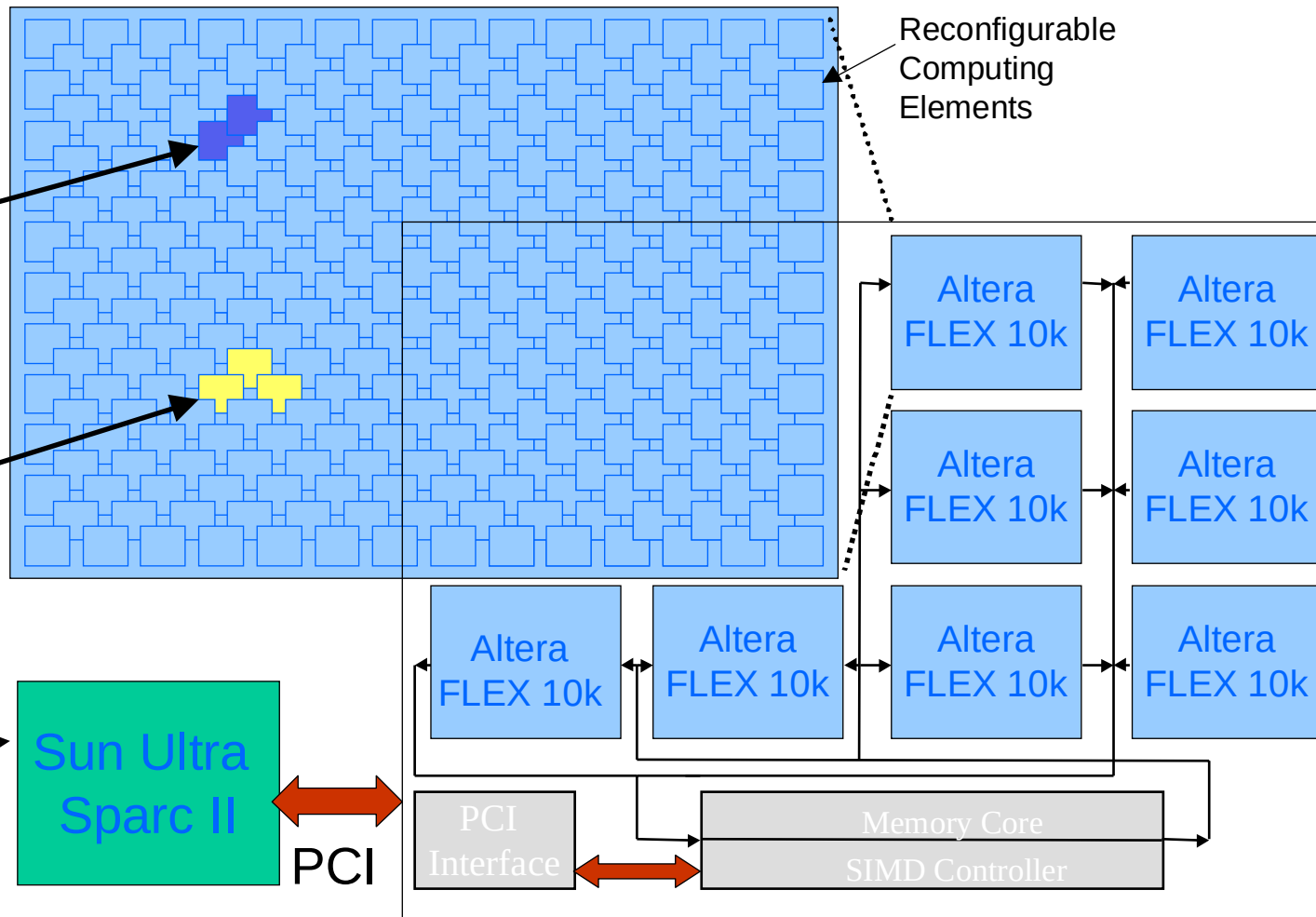
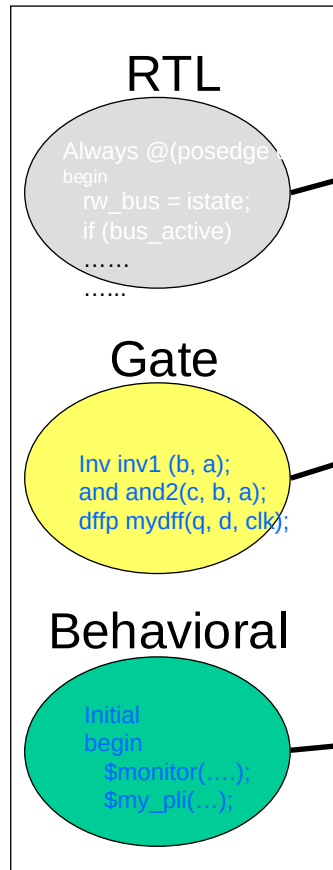
Sun Microsystems
Ultra-60
Workstation

Xcite-2000 System

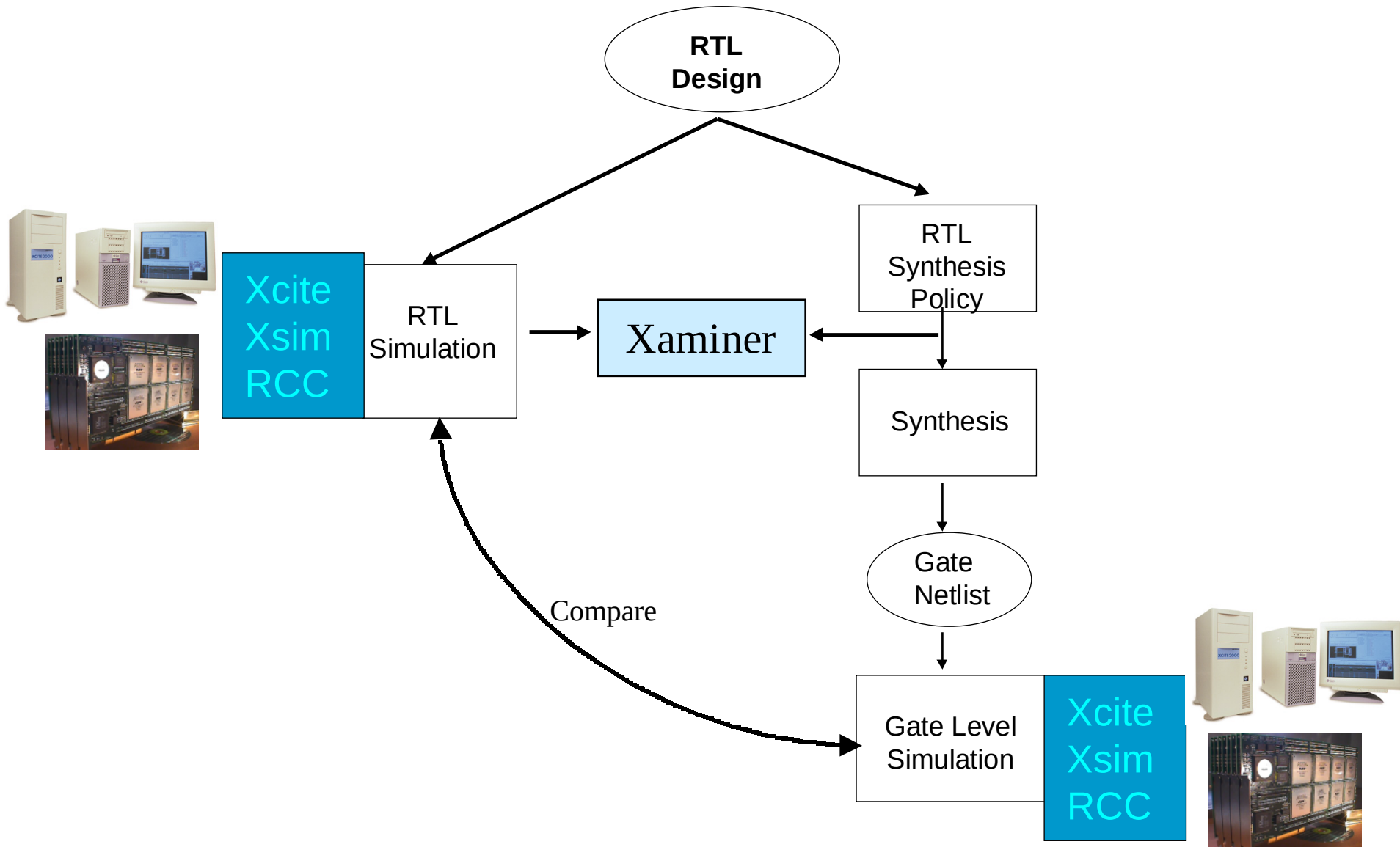


ReConfigurable Computing (RCC) Co-processor Architecture

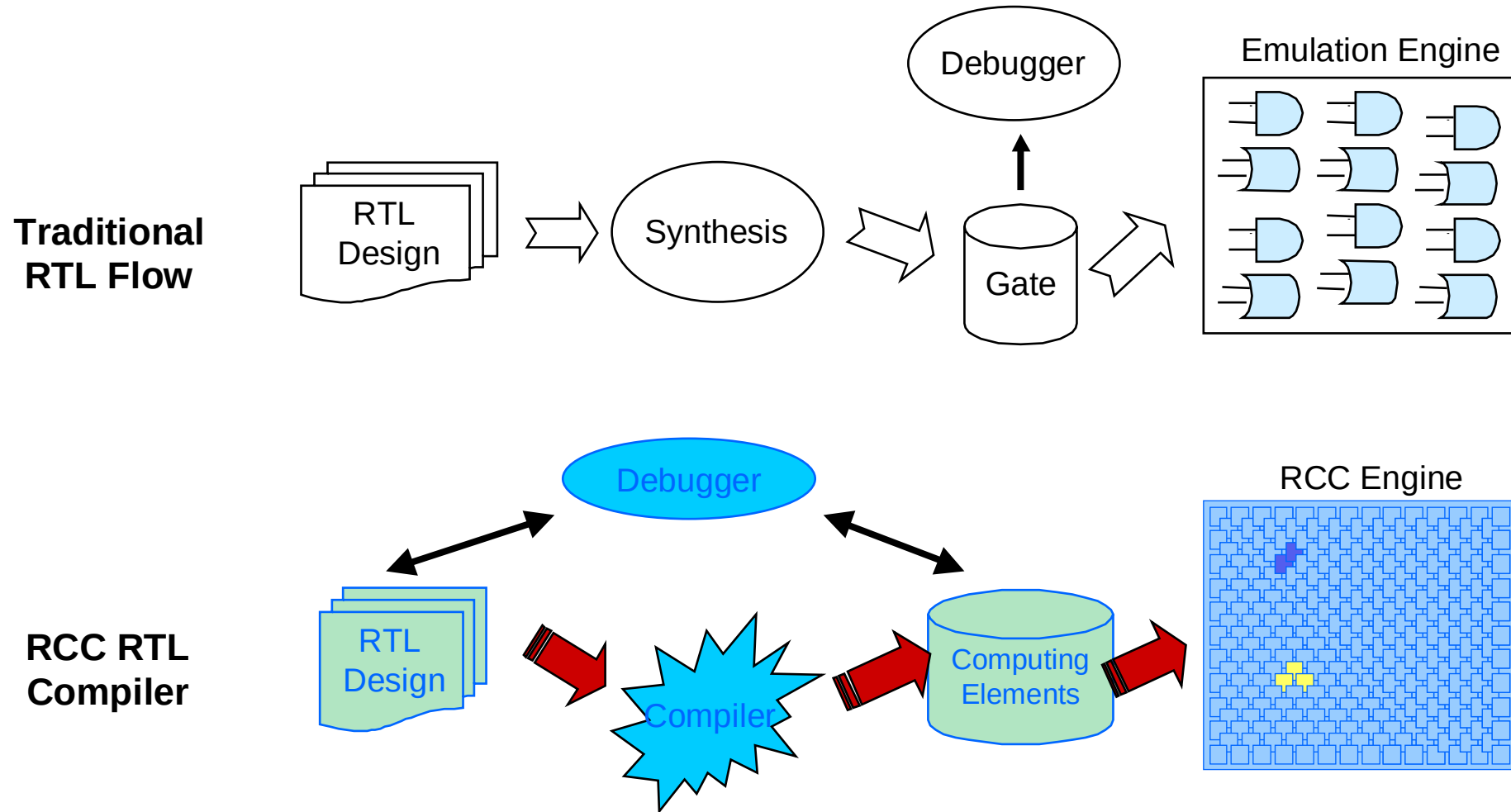
Verilog Design



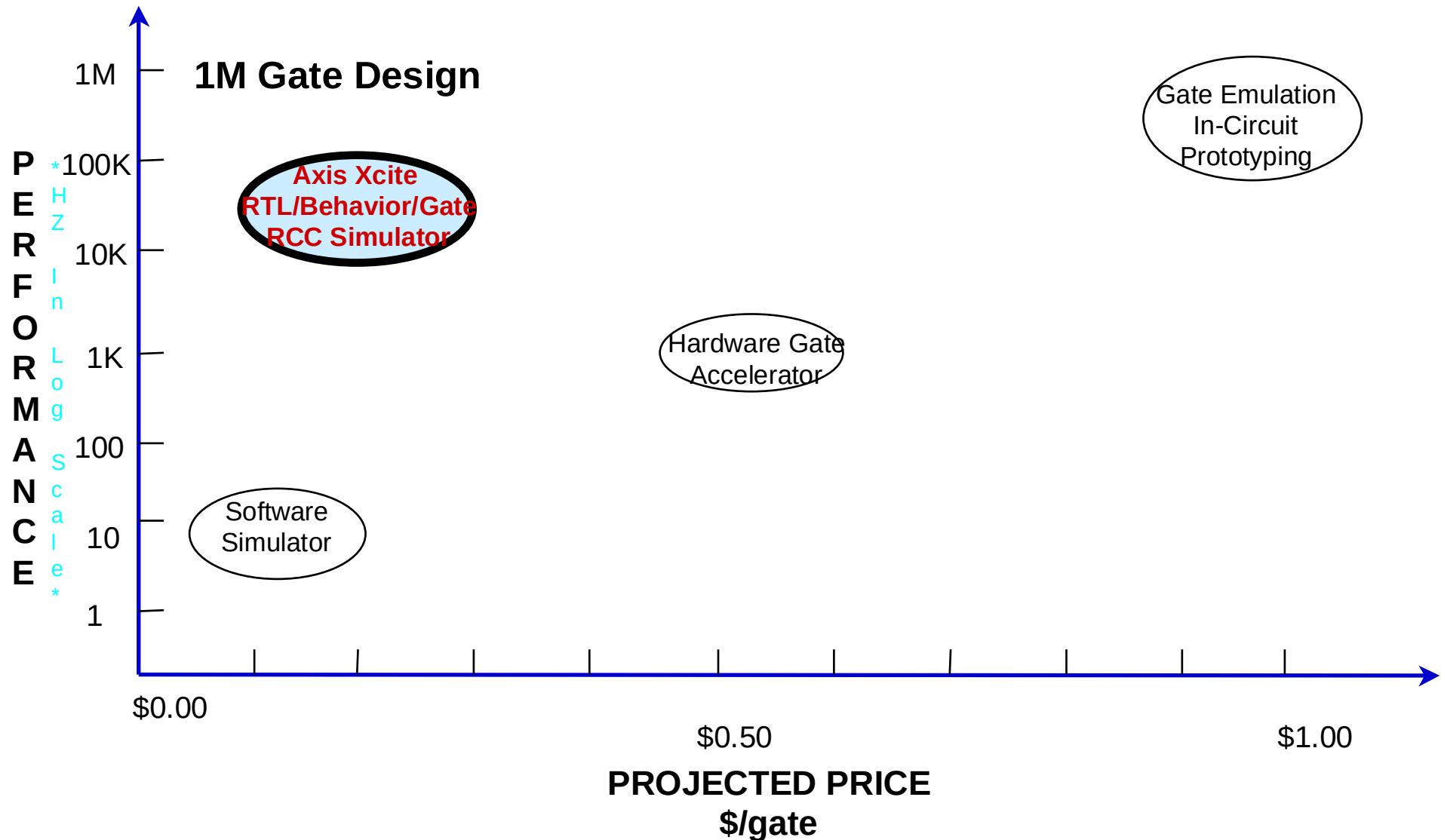
RTL Simulation Methodology



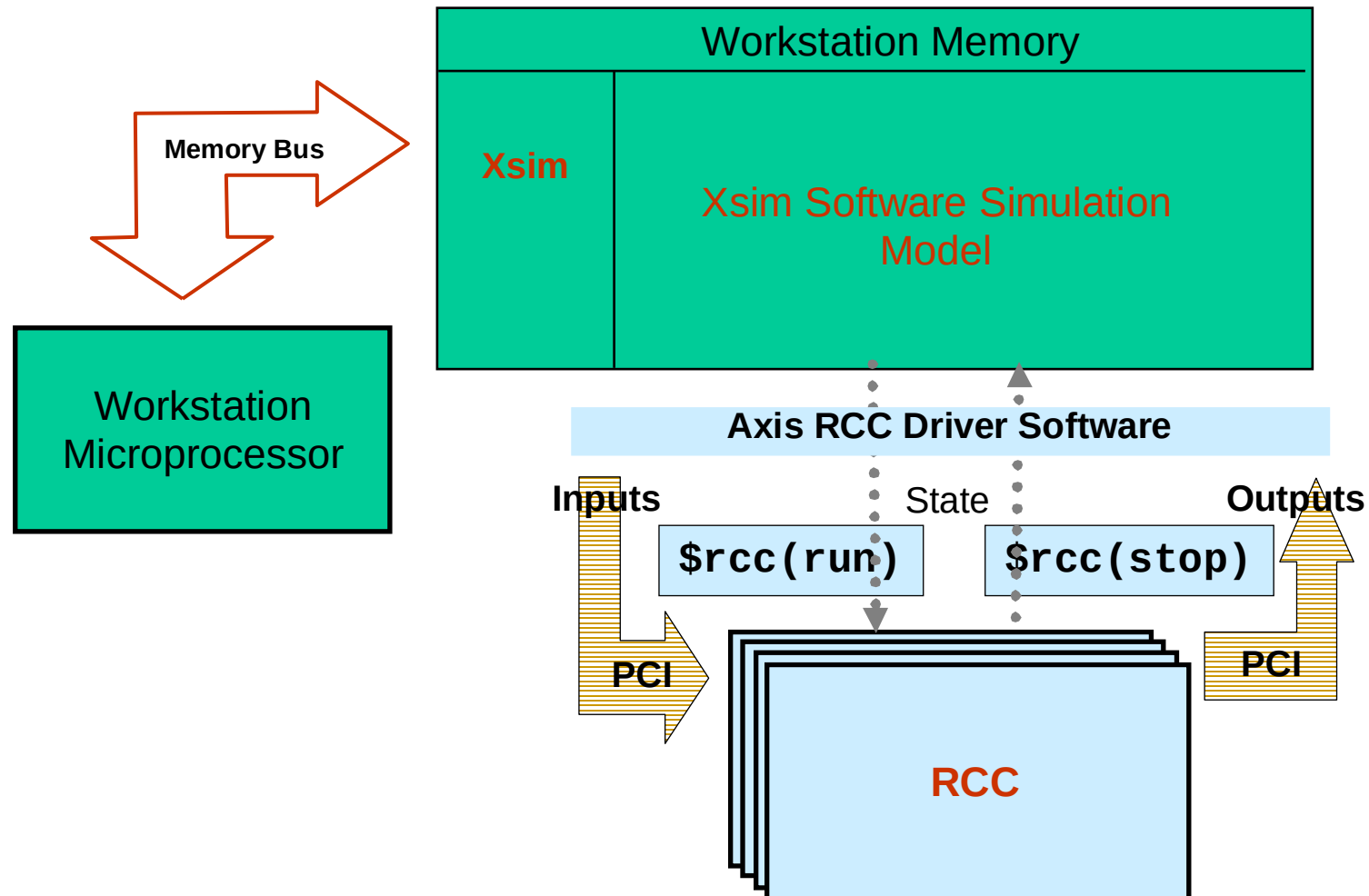
Xcite Direct RTL Compilation



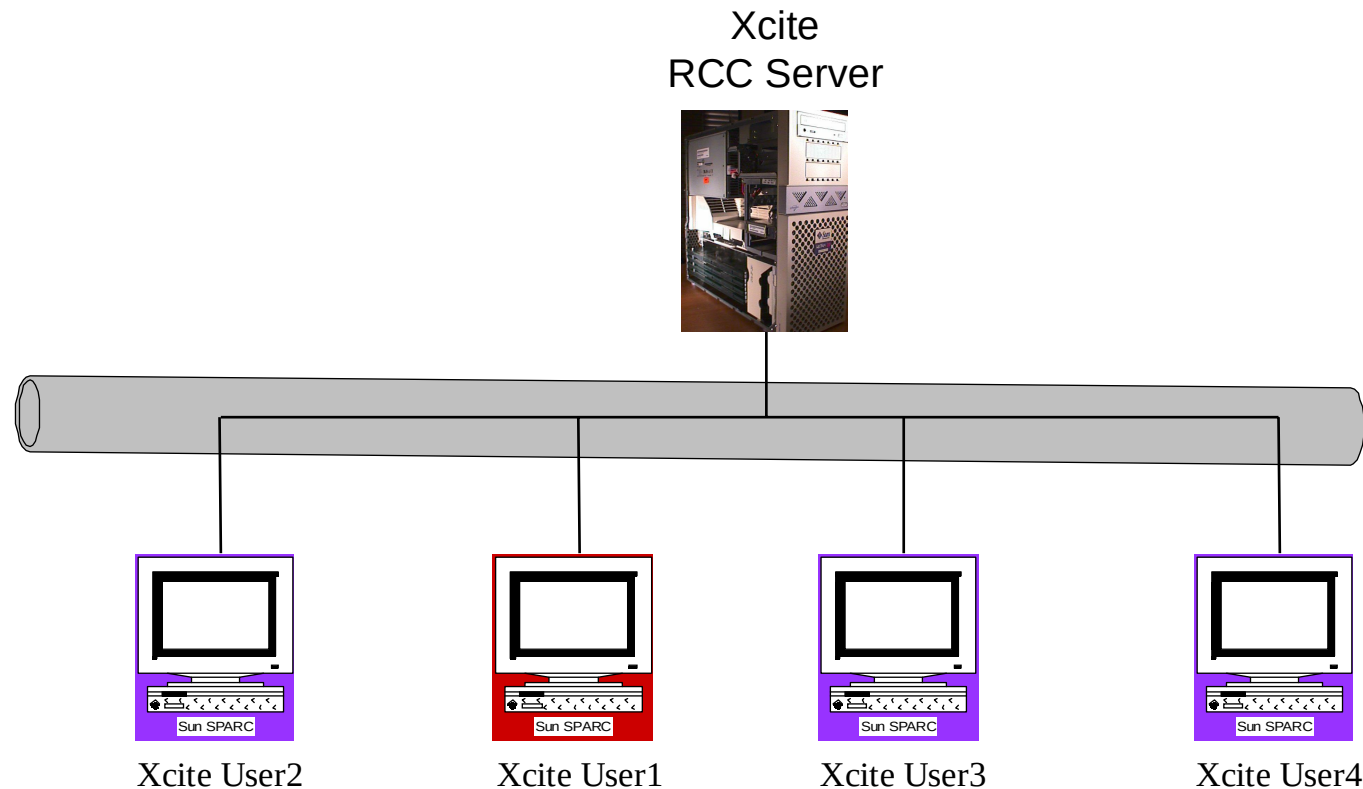
Verification Tools Landscape



Instantaneous Simulation Swap



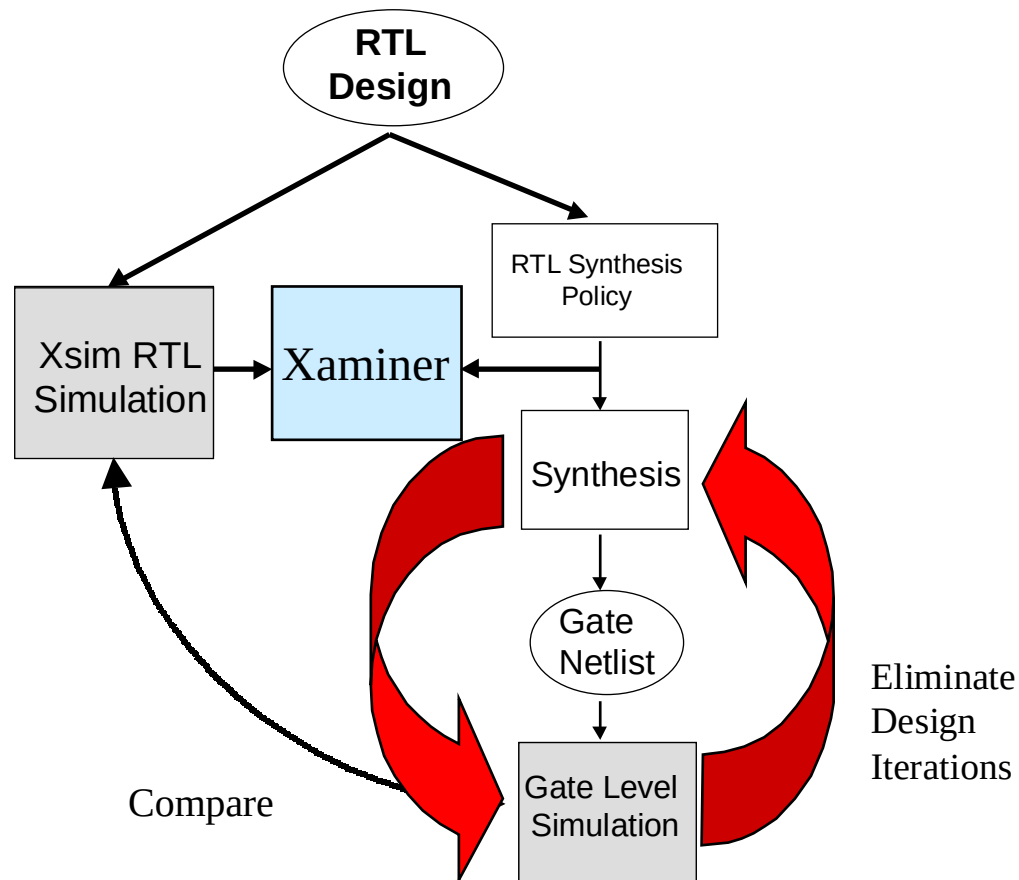
Sharing Xcite-1000 in a Engineering Design Team



©Verify99

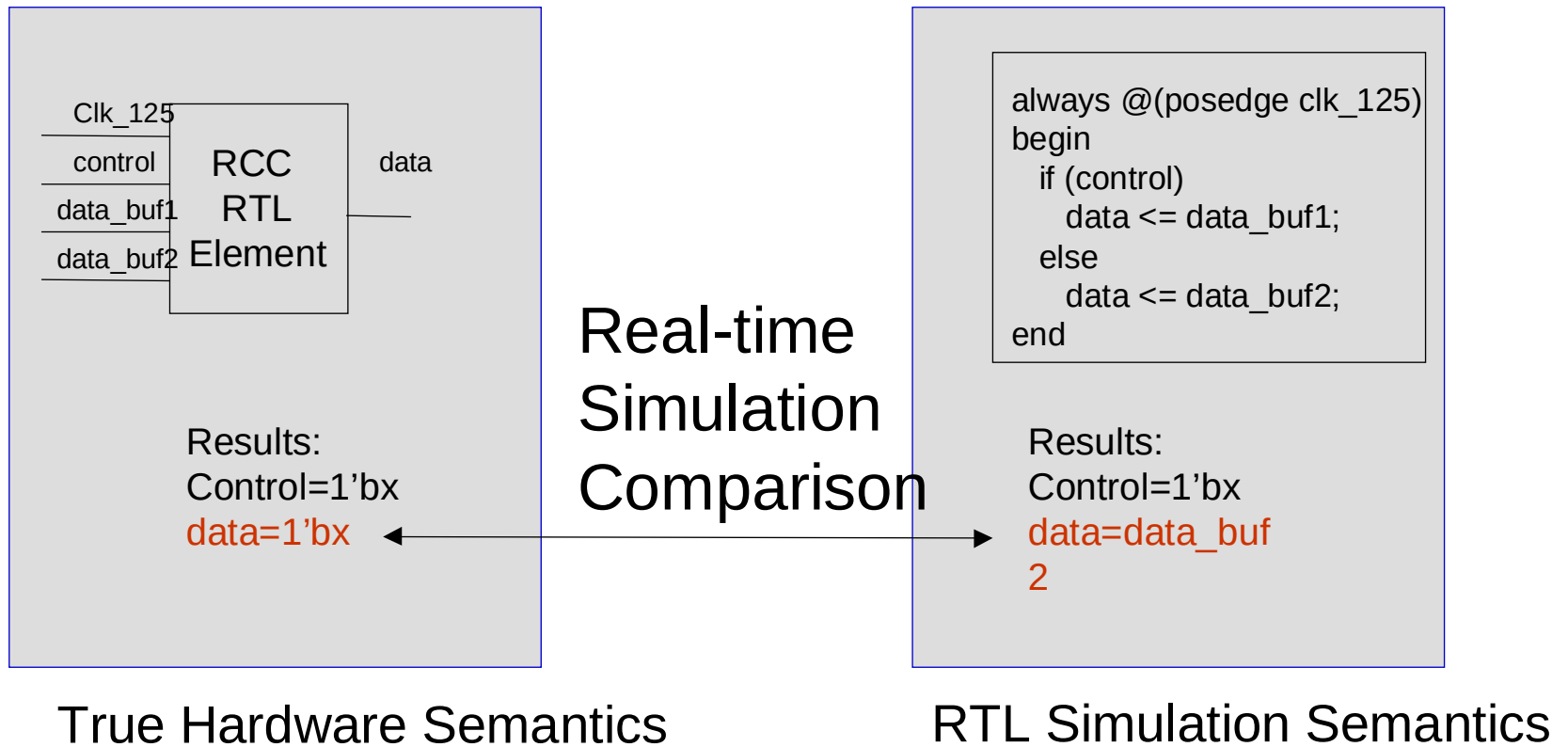
	Debugging using Xcite compiled simulator (Xsim)
	Running Xcite RCC

Xcite Xaminer Achieving Functional Closure



- Isolate gate level problems due to synthesis pragmas at RTL level
(論理合成のpragmaにより発生するゲートレベルでの問題をRTLで検出)
- Eliminate costly synthesis iterations to obtain functional closure.
(論理合成のイタレーションを削減)
- Automated problem detection during Xsim simulation with existing user testbench.
(ユーザーのテストベンチを用いてXSIM上で動作し問題発見)

Xcite Xaminer



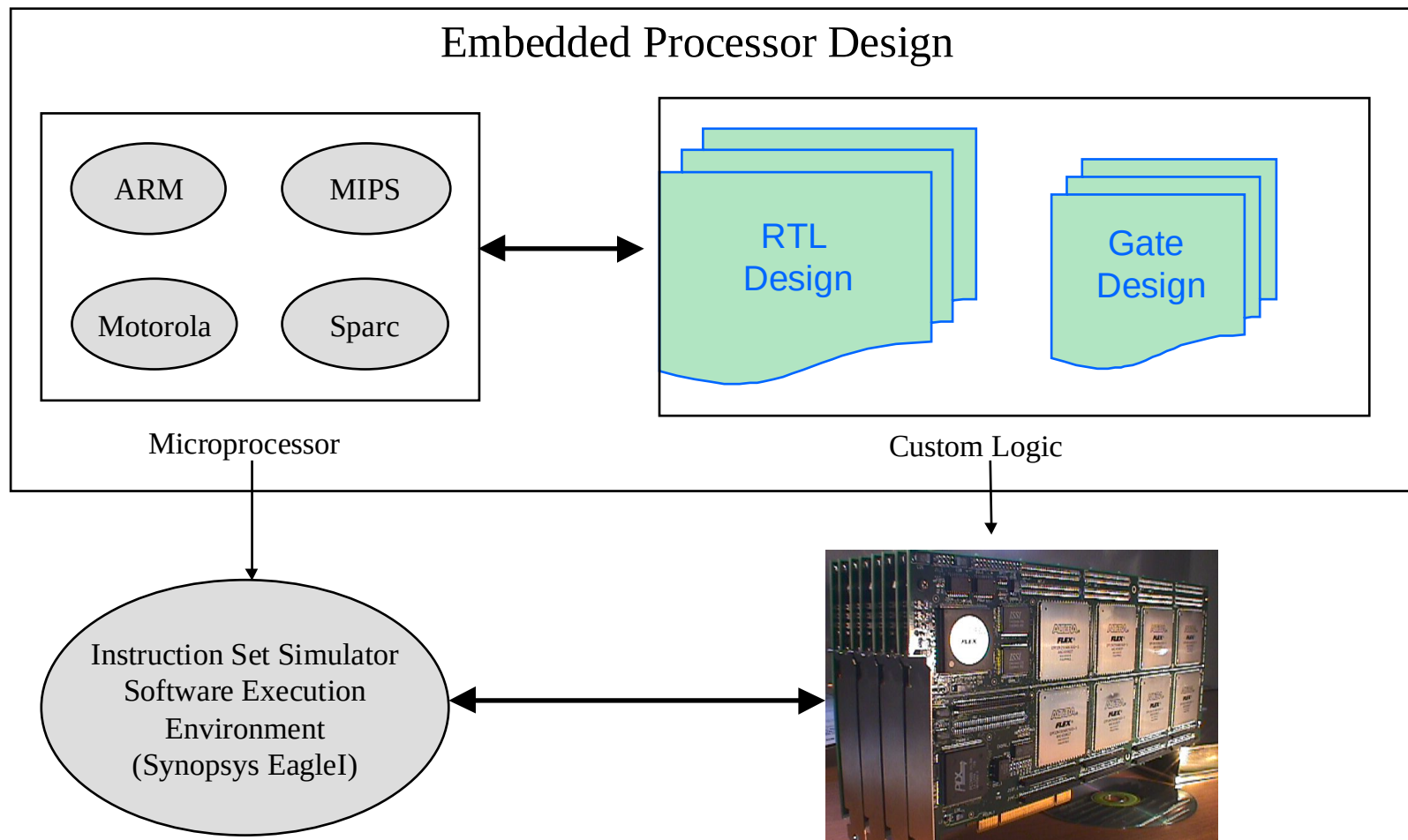
Xaminer Detection Examples

- ◆ Parallel case directive violation
- ◆ Full case directive violation
- ◆ Race condition detection
- ◆ Proper reset sequence not exercised
- ◆ Verilog functions not returning default values
- ◆ True X state RTL propagation

Xcite 2000 Benefits

- ◆ Up to 10 Million gate capacity in new external enclosure
- ◆ Small form factor (Same size as Sun desktide enclosure). One PCI extender cable connects workstation to RCC external box
- ◆ Up to 192M bits on-board RCC memory
- ◆ Up to 4G Bytes of hardware memory mapped onto Sun Ultra workstation.
- ◆ High performance simulation of 10K - 100K cycles per second

Hardware/Software Co-Simulation

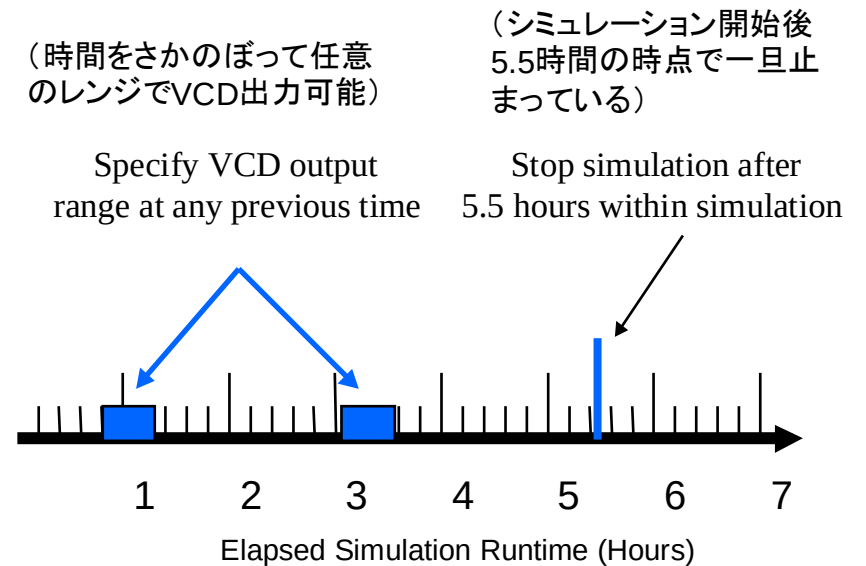


VCD On-Demand

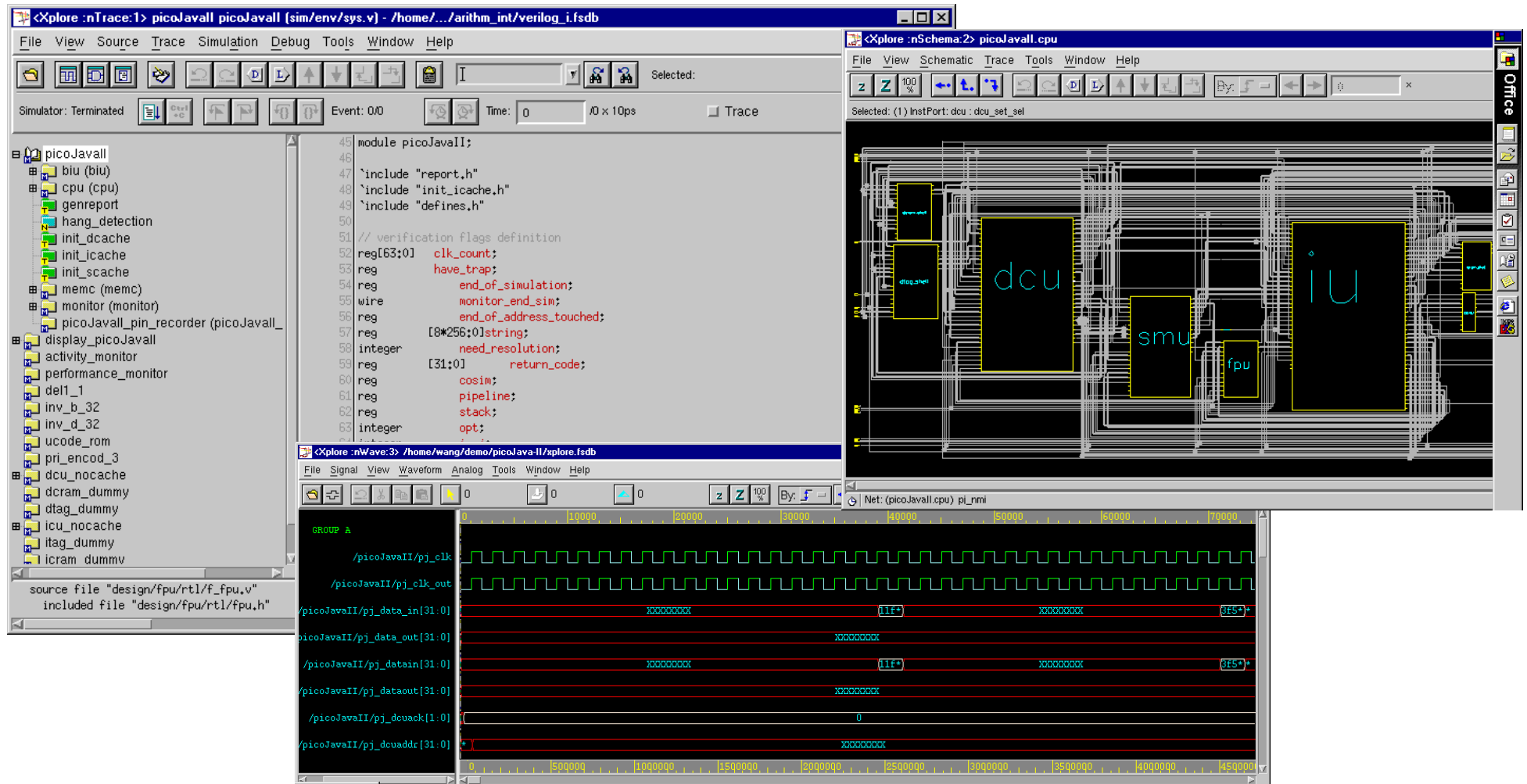
Xcite uses its proprietary technology to compress VCD data

(XciteはVCD dataを圧縮するために独自の技術を使っています。)

	Traditional Simulator	Xcite
Specification	Before Simulation	During Simulation
Hierarchy	One Hierarchy	Multiple Hierarchies
Performance	Reduce Simulation Speed	No Impact
Disk Storage 2M gate design	100GBytes for 1M cycles	1Mbyte for 1M cycles



Xplore Graphical Debug Interface



The Ultimate Verification System

Xcite

- ◆ Best Debugging Simulator - Xsim
- ◆ Fastest Simulator Using RCC Technology
10,000 to 100,000 cycles/sec
ReConfigurable Computing (RCC) Co-processor
- ◆ Advance Debugging Tools
 - Xaminer
 - VCD On-Demand
 - Instantaneous Simulation Swap
 - Xplore Graphical Interface
- ◆ Complete Hardware/Software Co-Verification Environment