Frontier Design

EDA Technofair 2000

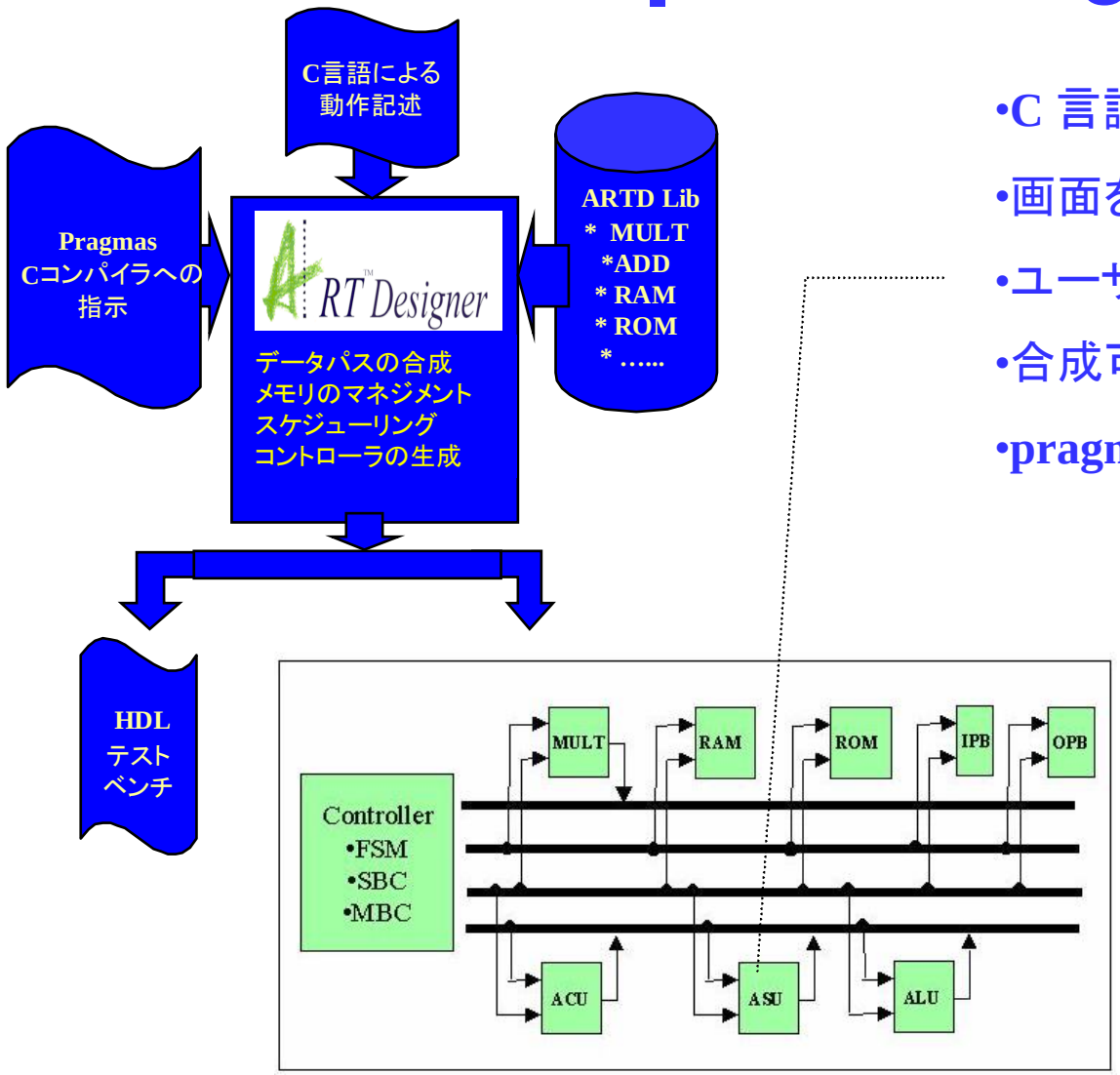
丸文株式会社
開発営業第2部
連絡先：TEL；03-3639-9640
imamura@marubun.co.jp

Frontier Design

A|RT Designer: From C to HDL

丸文株式会社
開発営業第2部
連絡先：TEL；03-3639-9640
imamura@marubun.co.jp

A|RT Designer

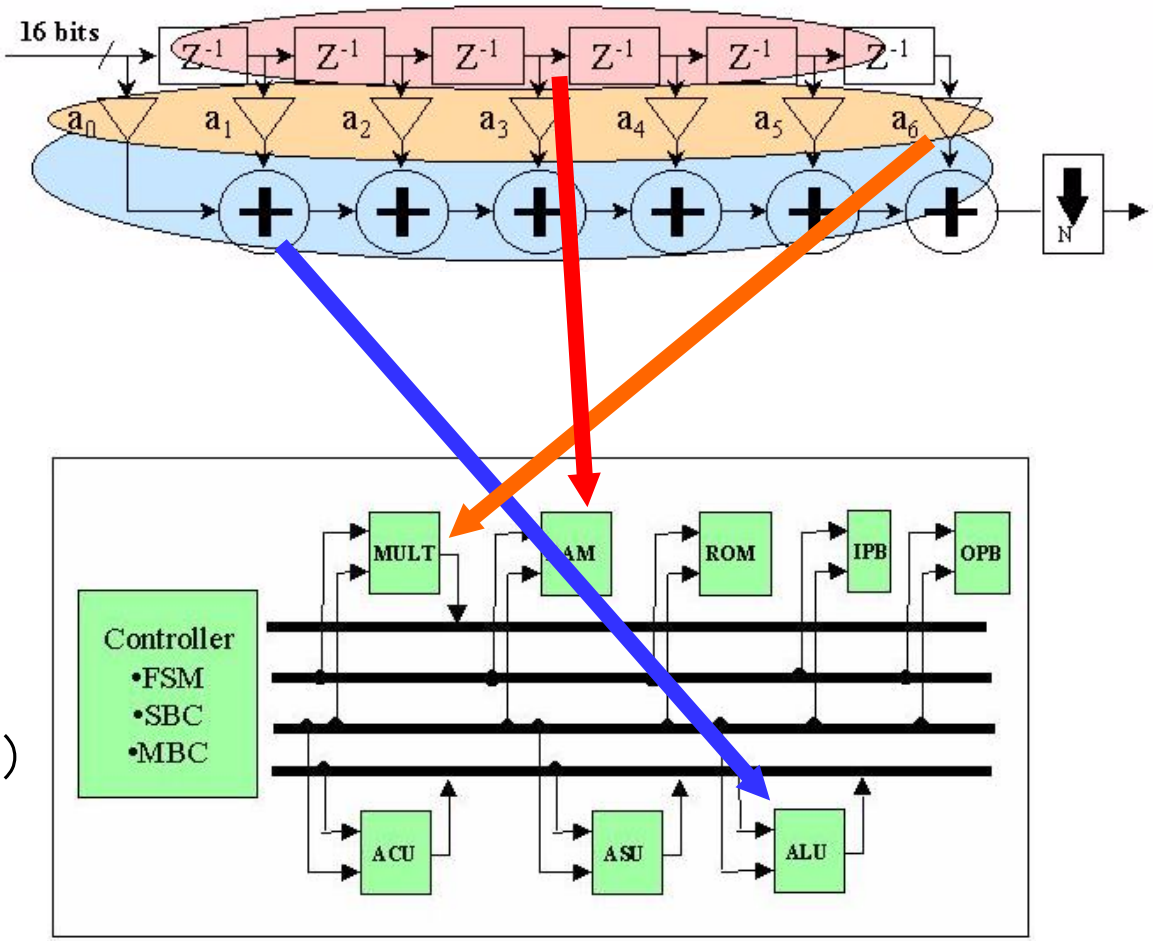


- C 言語記述を動作合成する最新ツール
- 画面を通して対話的に最適化を探求
- ユーザ設計のブロックが指定可能
- 合成可能なVHDL/Verilogを生成
- pragmaによって機能の指定が可能

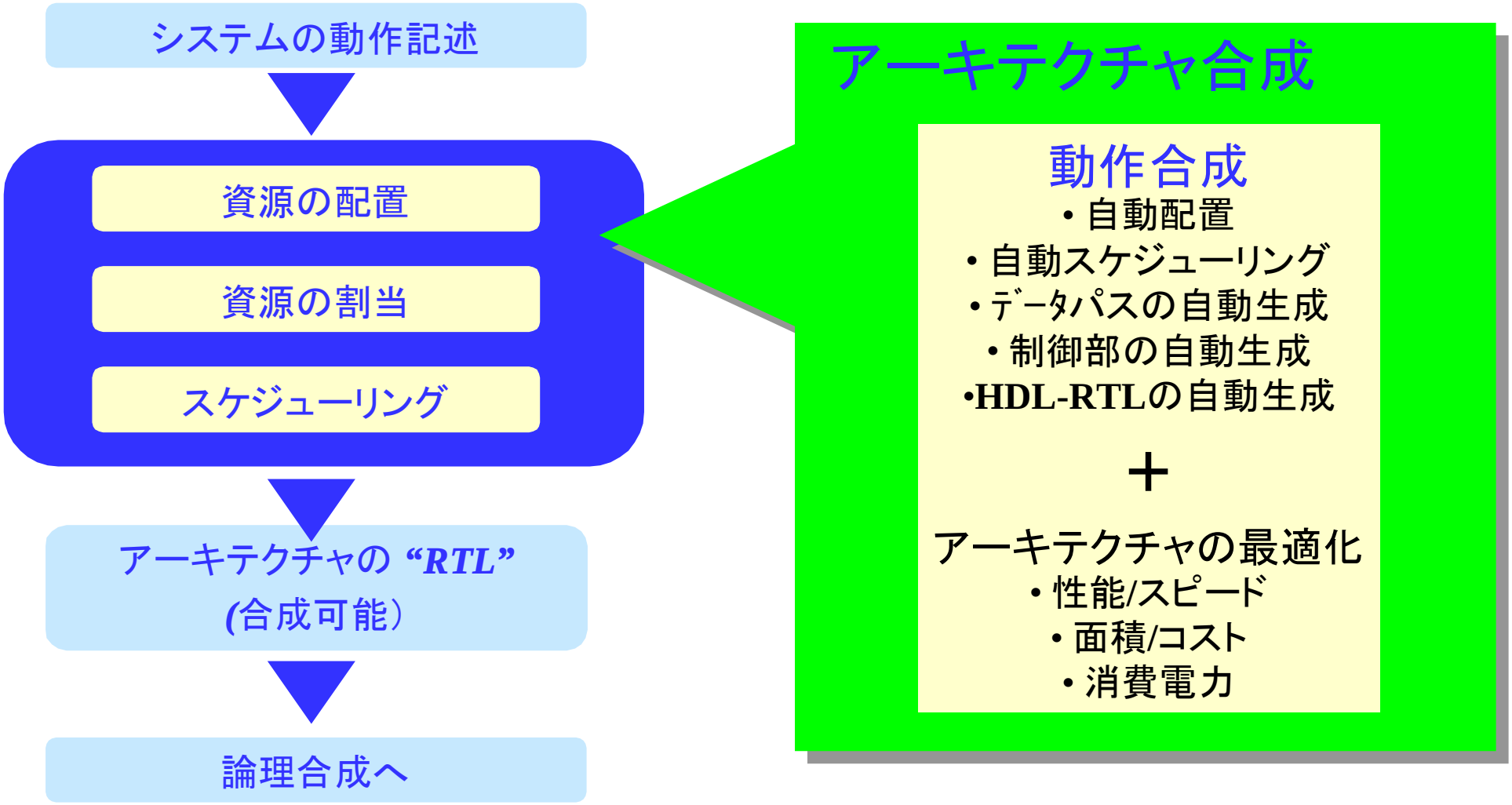
Frontier Design

動作記述からアーキテクチャを生成

- ビヘイビア/アルゴリズム
  - 動作,機能の記述
  - 入出力信号、ｻﾝﾌﾟﾙﾚｰﾄ
- アーキテクチャの生成
  - コントローラ
  - データパス
  - リソース
    - （ALU、ROM，RAM…）
  - クロック



最適なアーキテクチャを合成



資源の配置と割当

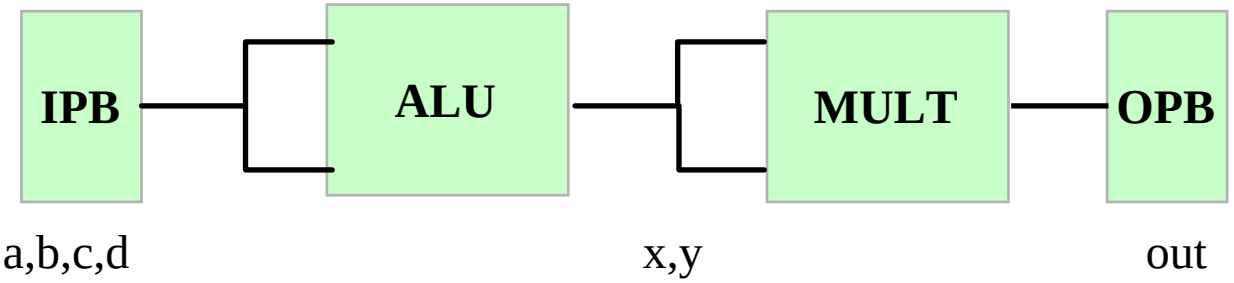
C-言語

```
x = a + b;
y = c - d;
out = x * y;
```

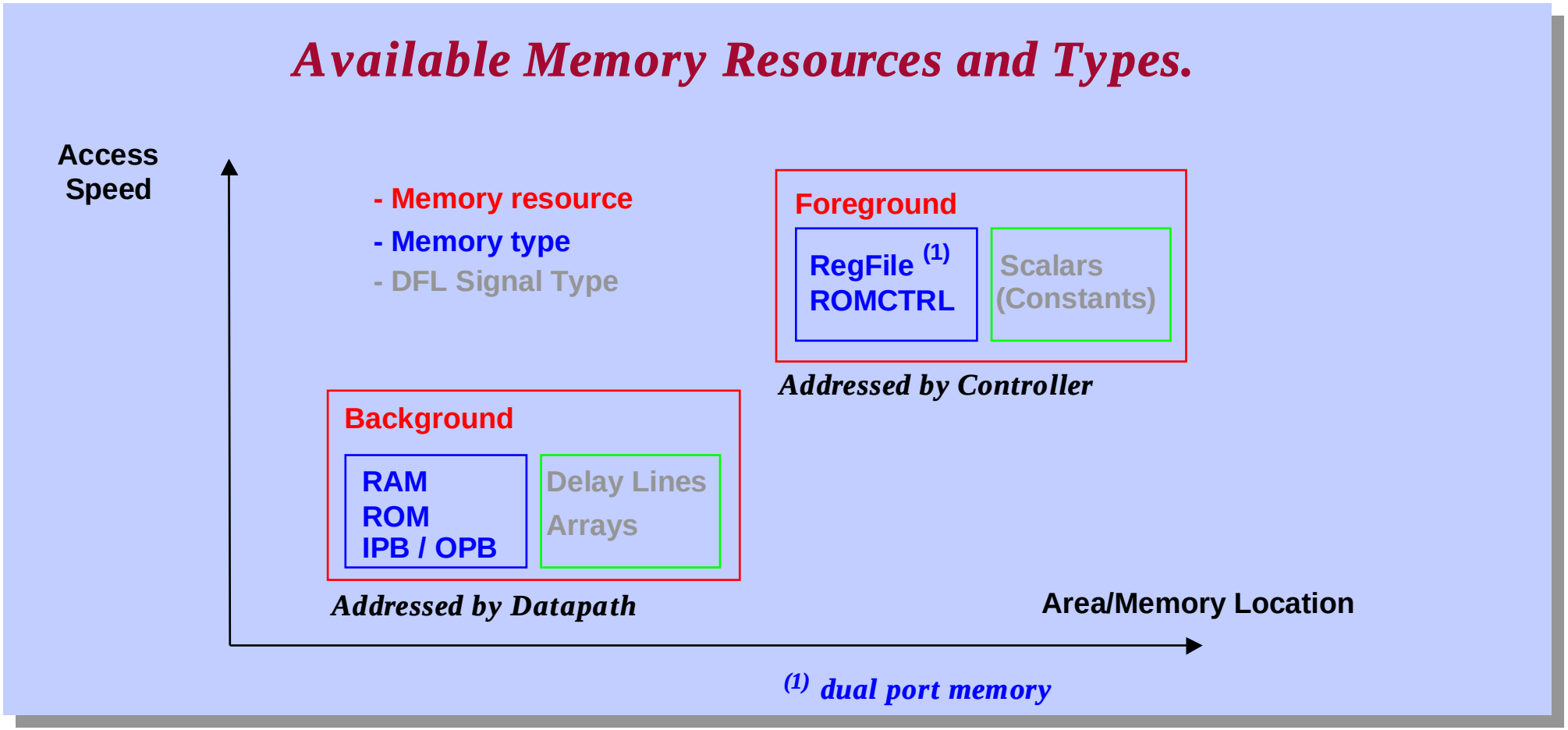
資源の割当と配置のルール

operation	EXU	mode
_*_	MULT	“mult”
_+_	ALU	“add”
:reg1-:reg2	ALU	“sub”
cast(_:reg1)	ALU	“pass”

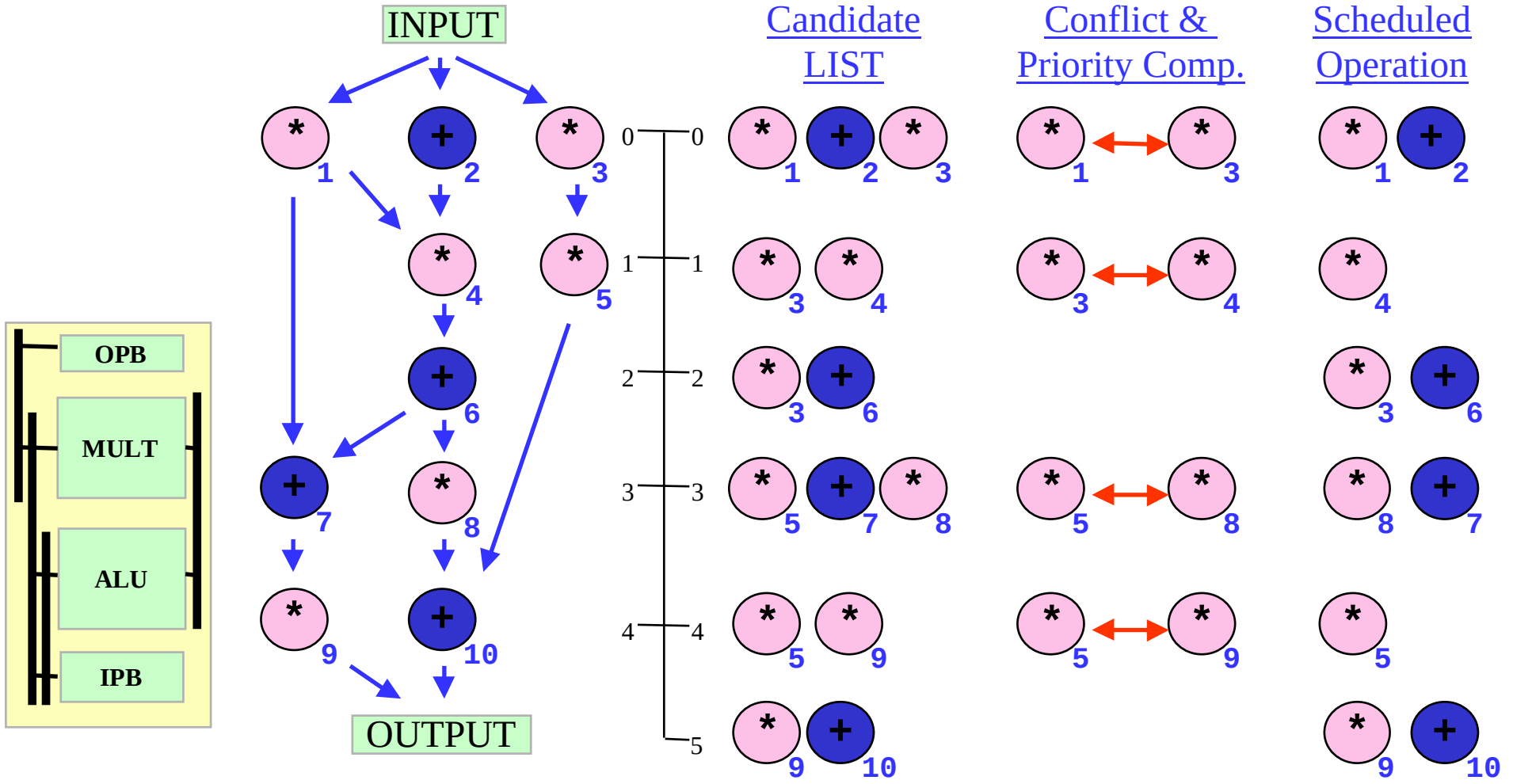
アルゴリズムのマッピング



メモリアーキテクチャの生成



スケジューリング

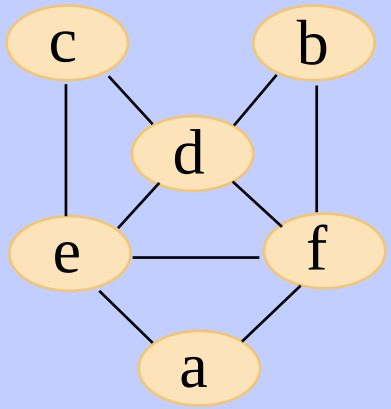


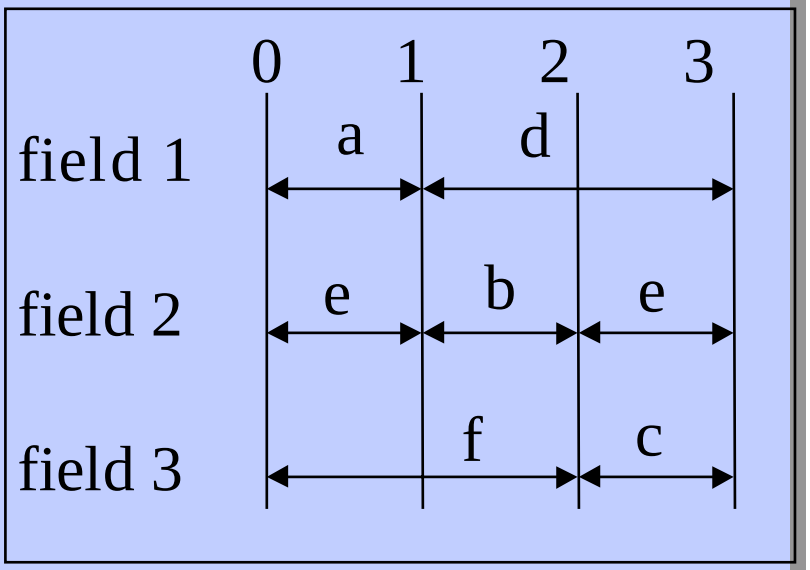
Frontier Design

スケジューリング ： レジスタの共有化

Register Assignment & Register Optimization.

variable	lifetime	conflict graph
a	[0,1]	
b	[1,2]	
c	[2,3]	
d	[1,3]	
e	[0,1] U [2,3]	
f	[0,2]	





スケジューリング：Loop Folding

- Faster Schedule Through more Parallellism
- MicroROM Area Increases (#potentials)
- Size of Register Files Increases
- Example

```
pot 0   s = 0;
        FOR i = 1 to 10 {
pot 1       p[i] = c[i]*in[i];
pot 2       s = s+p[i];
        }
```

21 cycles

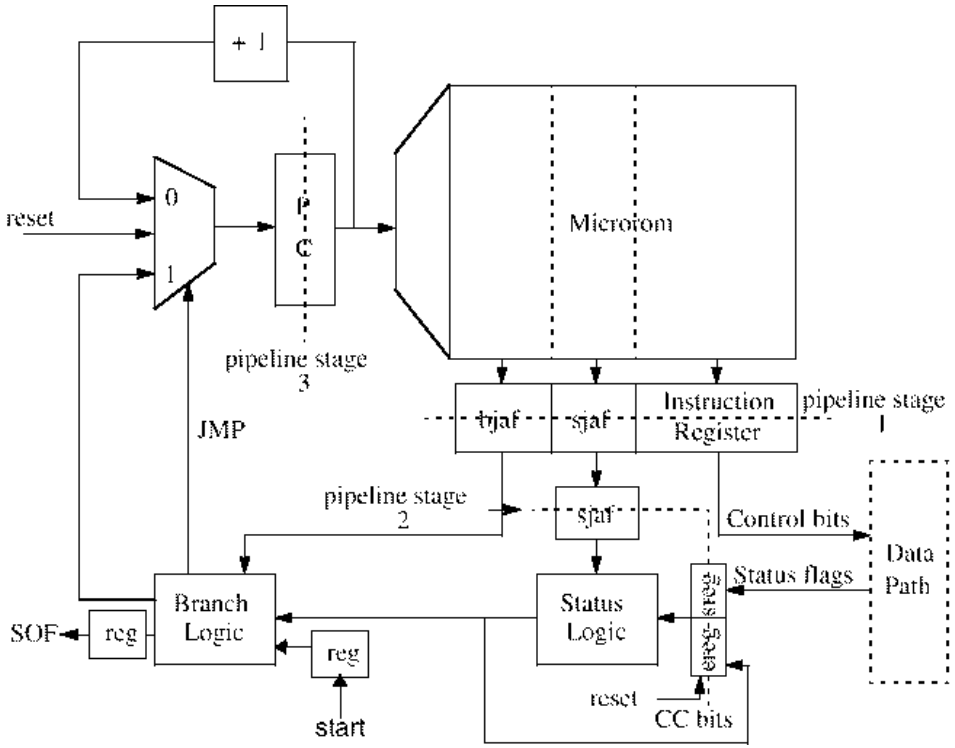
Loop Folding

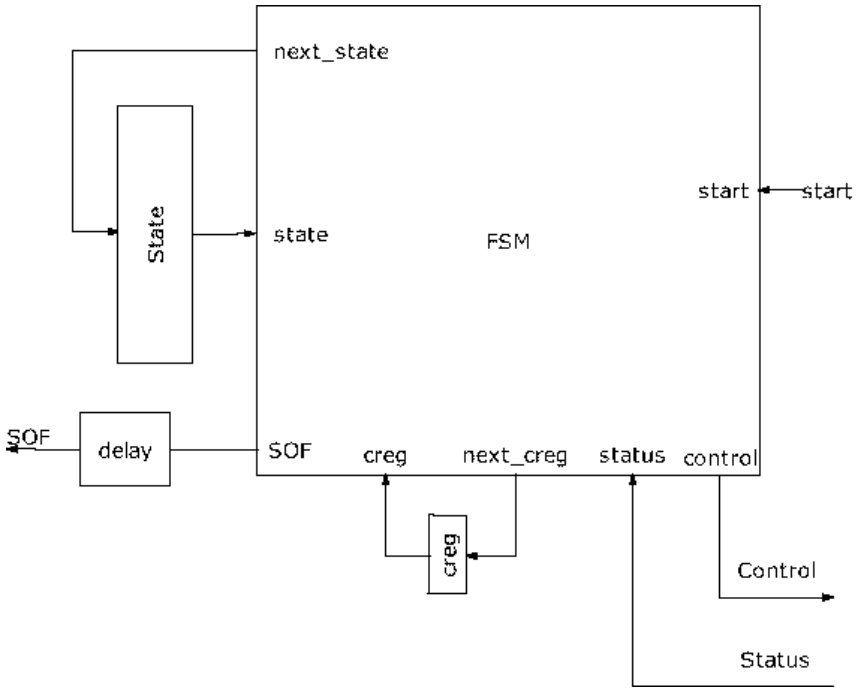
```
pot 0   s = 0;
pot 1   p[1] = c[1]*in[1];
        FOR i = 2 to 10 {
pot 2      s = s+p[i-1];p[i] = c[i]*in[i];
        }
```

12 cycles

コントローラの生成

- **User can choose from 6 possible controller architectures.**

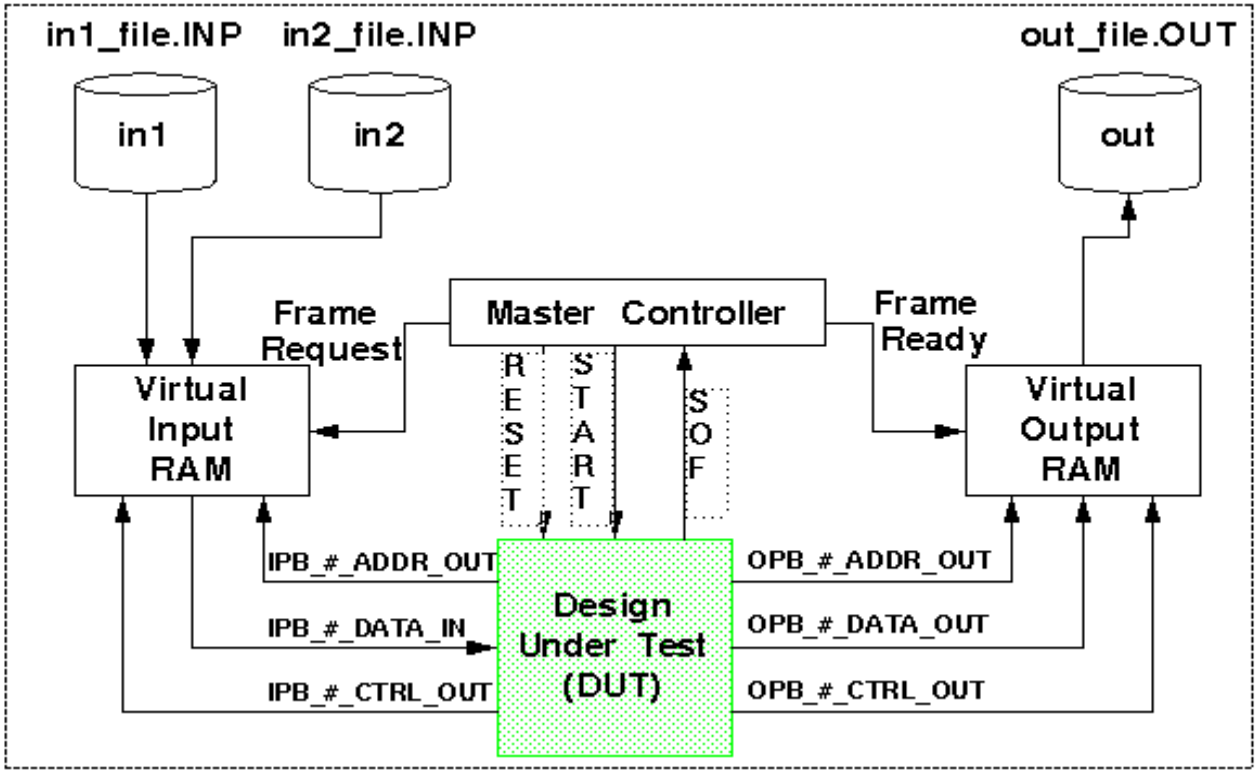




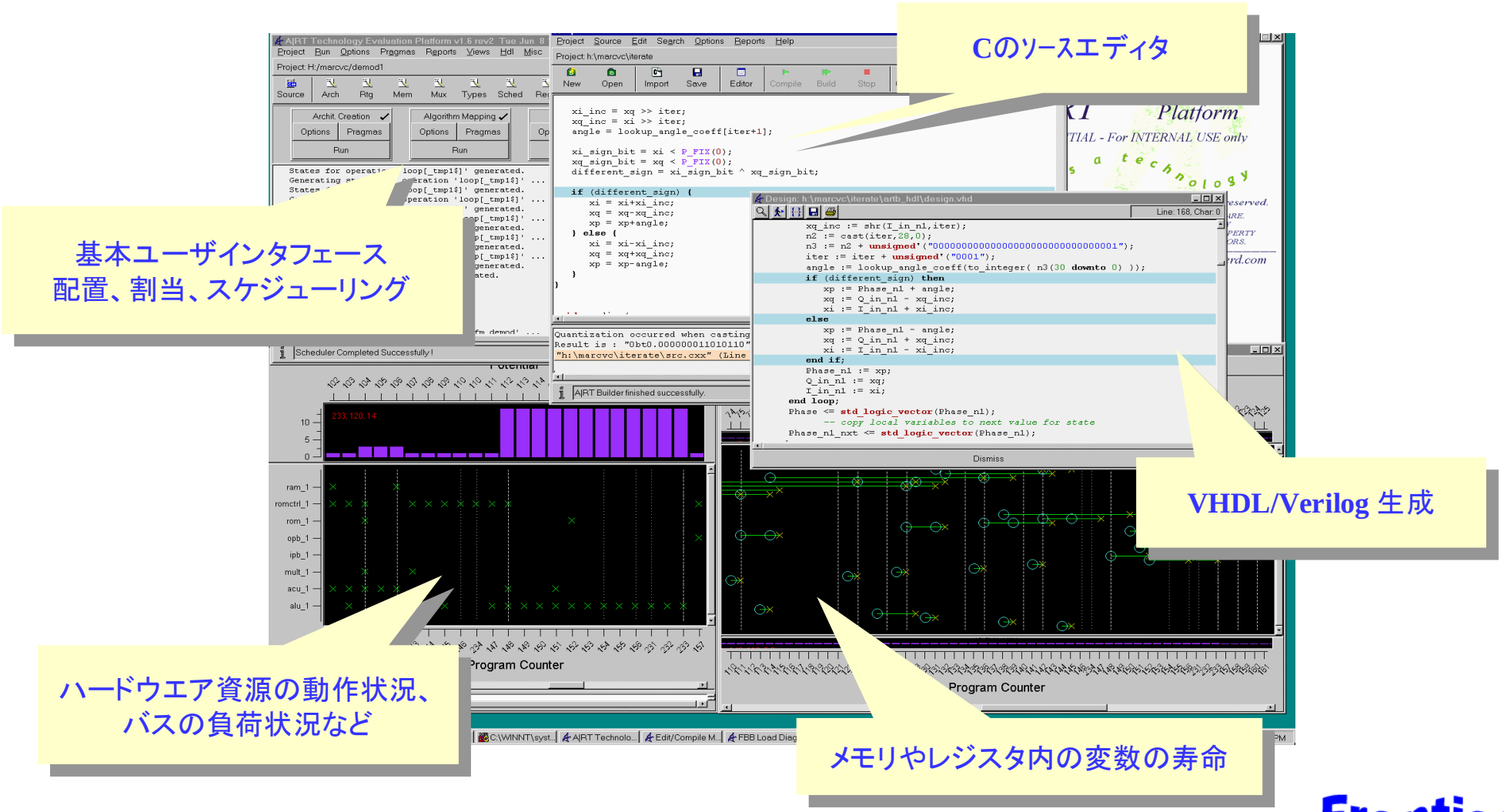
Frontier Design

RTL-HDL(ネットリスト)の生成

- Synthesizable VHDL or Verilog
- Processor Netlist
- Testbench



対話型設計と最適化の探求



A|RT Designerの特徴

- C-based behavioral synthesis tool. Offers true “Algorithm to RTL” solution
- No ‘blackbox’ tool. By using pragmas the user has full control over:
  - datapath composition (arithmetic, memory, IO, address / databusses..)
  - operation assignment
  - scheduling & register generation
  - controller design : choose from 6 possible controllers
- Very fast. Facilitates extensive “what-if” analysis at the architecture level.

A|RT Designer の特徴(2)

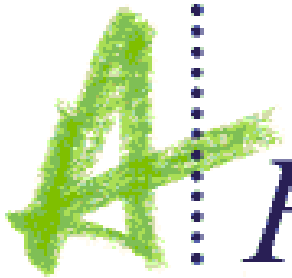
- Allows to synthesize a customized datapath & controller for an algorithm specified in C
- ART Designer generates an algorithm specific processor with a user defined instruction set.
  - The ultimate in flexible instruction set processors
  - Beyond approaches such as ARC, Tensilica, etc..
- ART Designer is an open system. Allows to add new instructions and datapath elements to the library
- Runs on PC/NT and Workstation

A|RT Designer の応用例

- Design of co-processors for compute intensive tasks in a SOC design
- Implement high performance algorithms on FPGA
- Ultra low power DSP ASIC Design
- Migration of DSP processor based solutions to high performance FPGA solutions.
- Reconfigurable computing

Frontier Design

http://www.frontierd.com



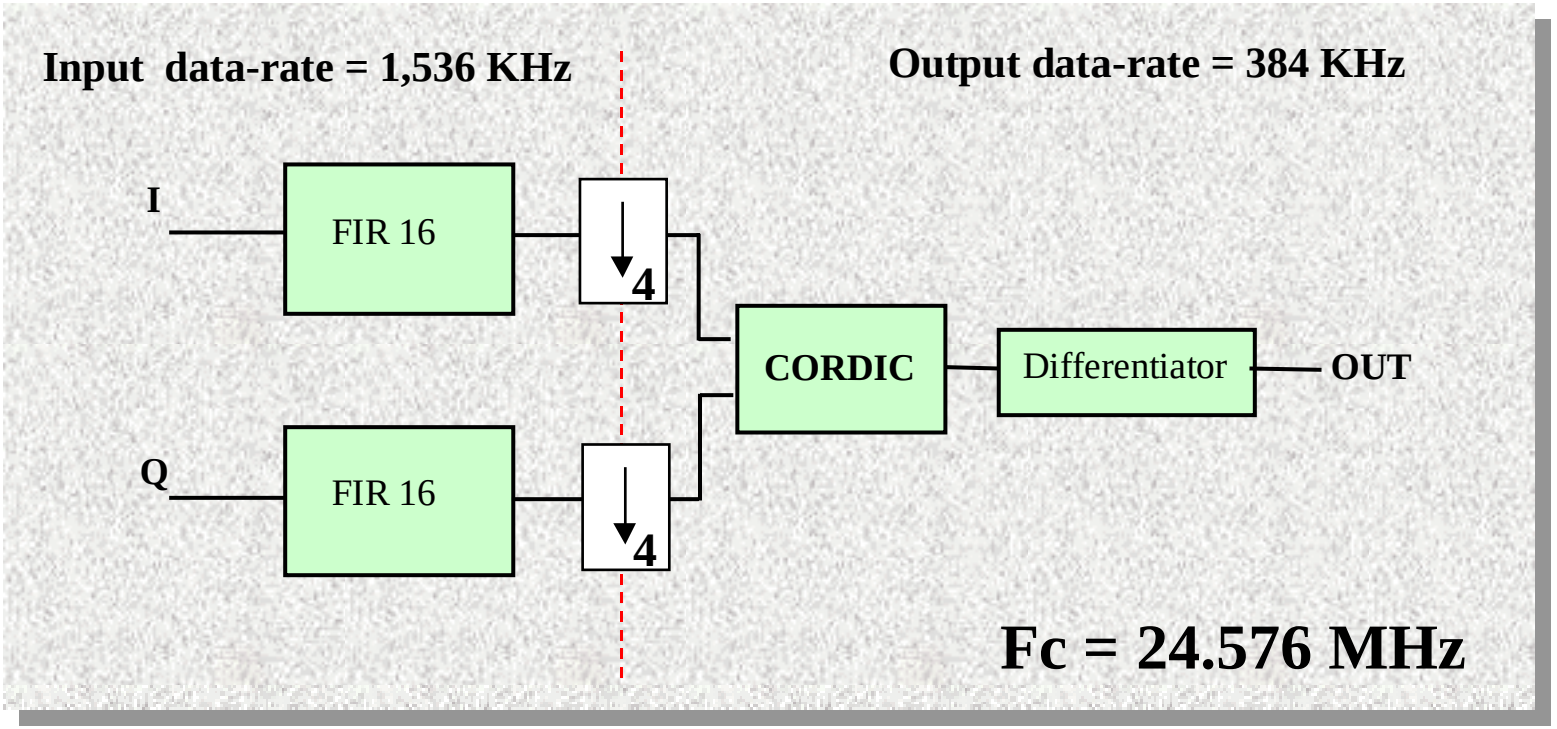
ART™ Designer

- 応用例: FM demodulator -

丸文株式会社
開発営業第2部
連絡先：TEL；03-3639-9640
imamura@marubun.co.jp

Case Study

FM復調器のアルゴリズム



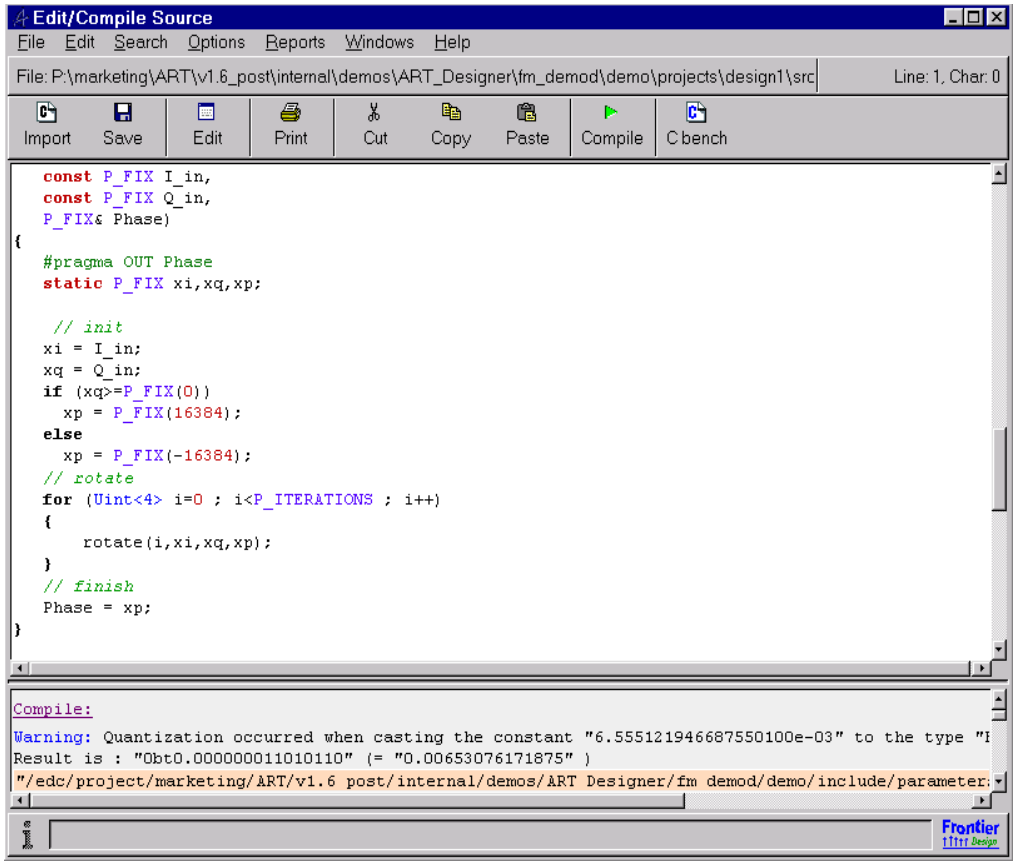
$$\frac{24.576\text{MHz}}{384\text{KHz}}$$

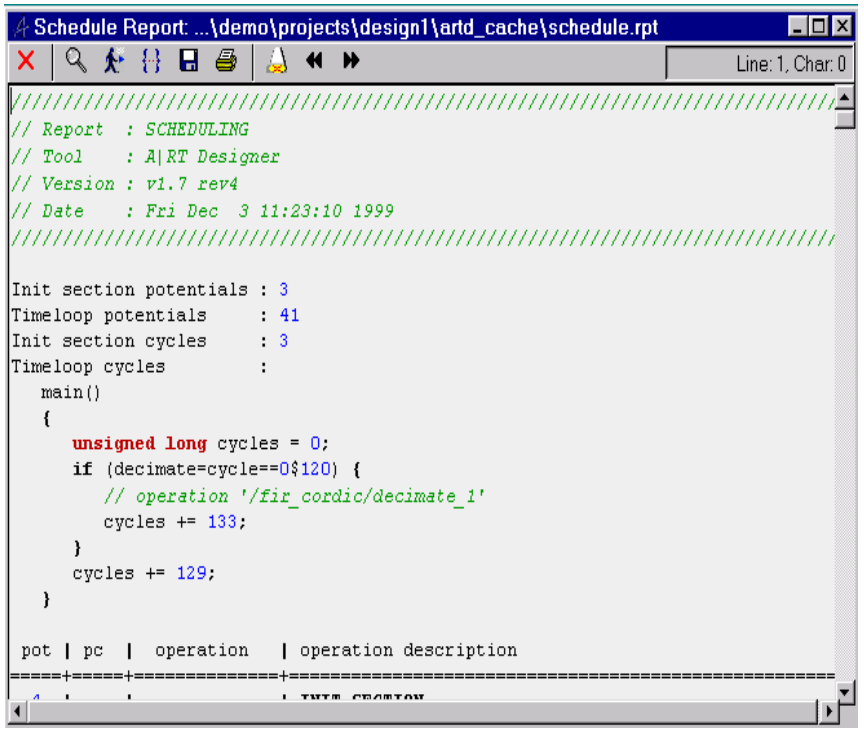
設計目標

64 cycles to compute every output

Case Study

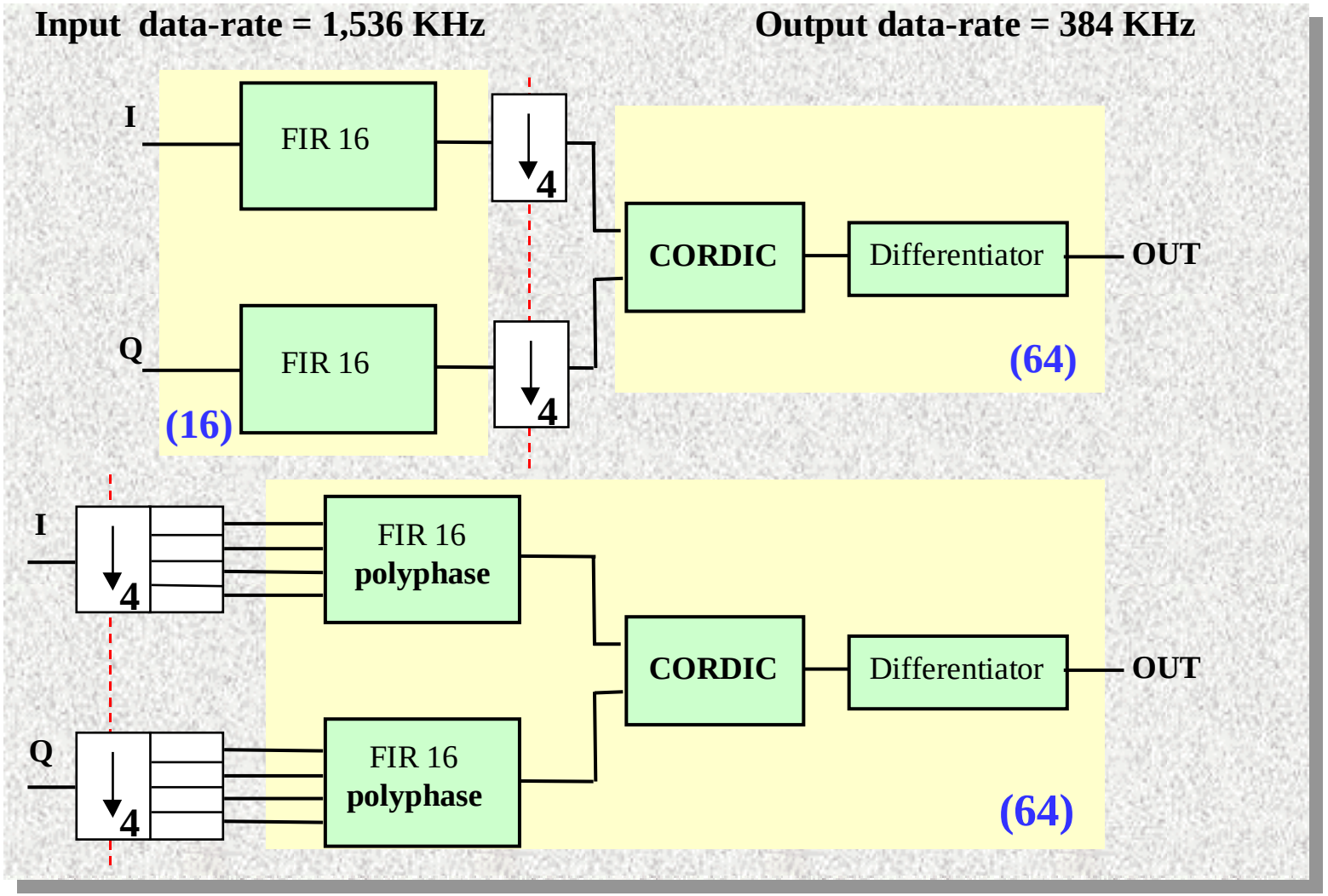
デフォルト設定での結果





129 cycles for filtering
133 cycles for cordic

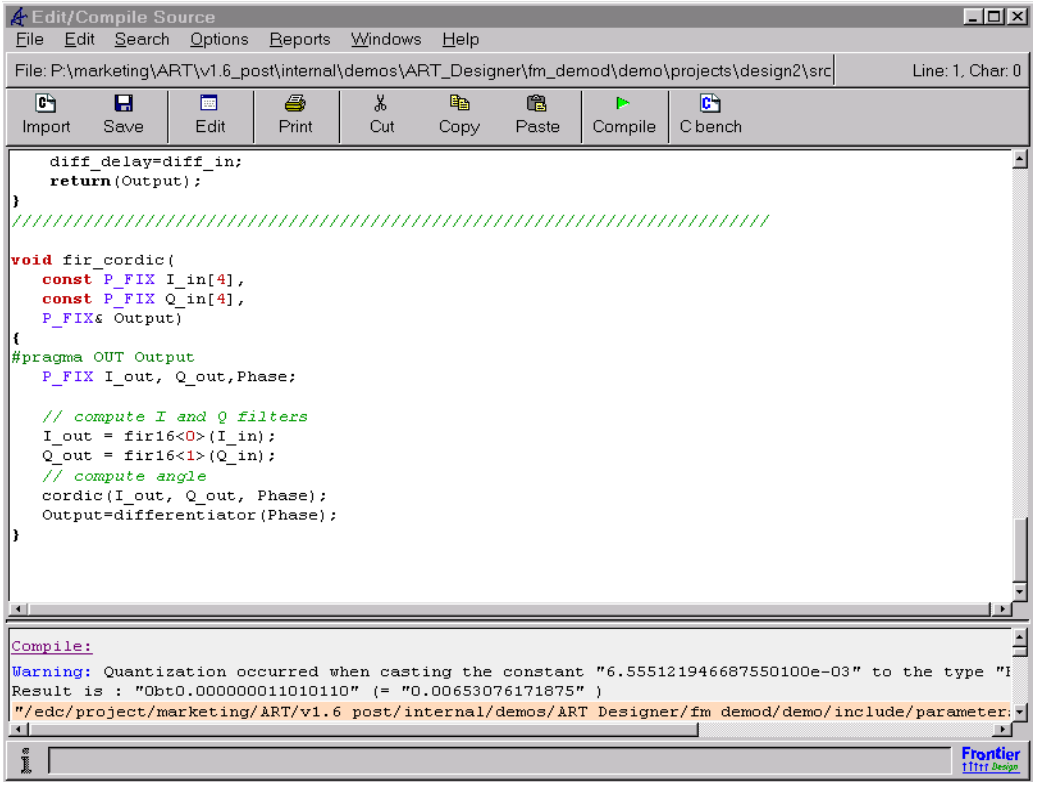
アルゴリズムの変更

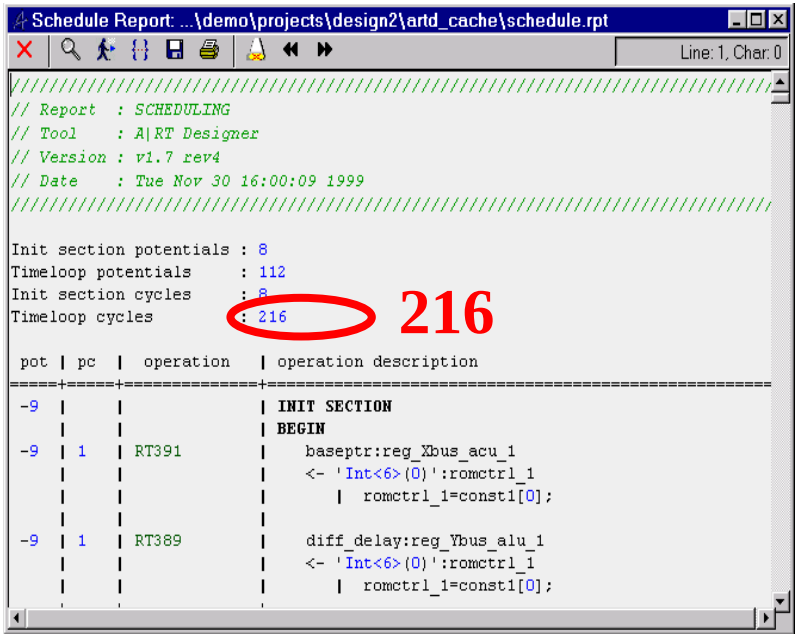

Input data-rate = 1,536 KHz
Output data-rate = 384 KHz
I
FIR 16
4
CORDIC
Differentiator
OUT
Q
FIR 16
4
(16)
(64)
I
4
FIR 16
polyphase
CORDIC
Differentiator
OUT
Q
4
FIR 16
polyphase
(64)

Case Study

アルゴリズムの変更

-ポリフェーズフィルタの使用結果-



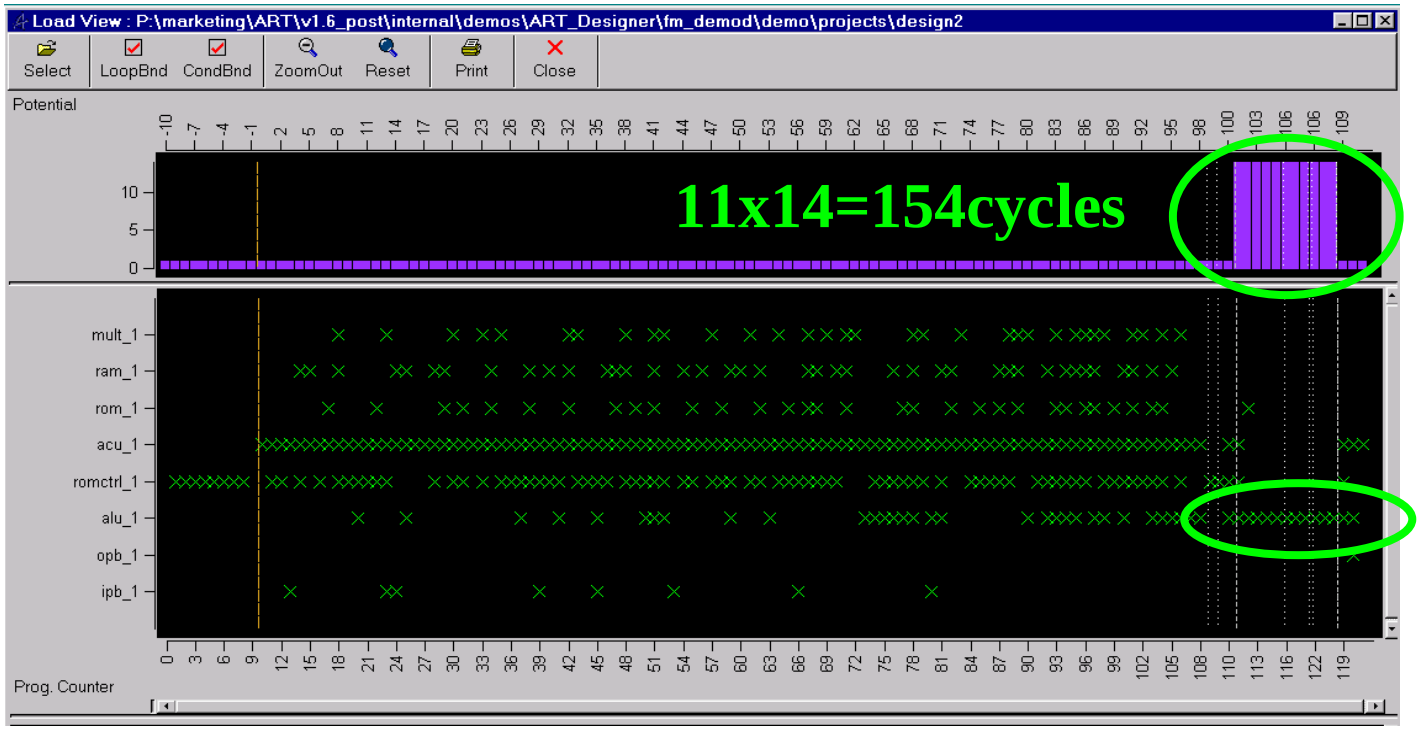


Frontier Design

Case Study

専用ユニット（ASU）の割当

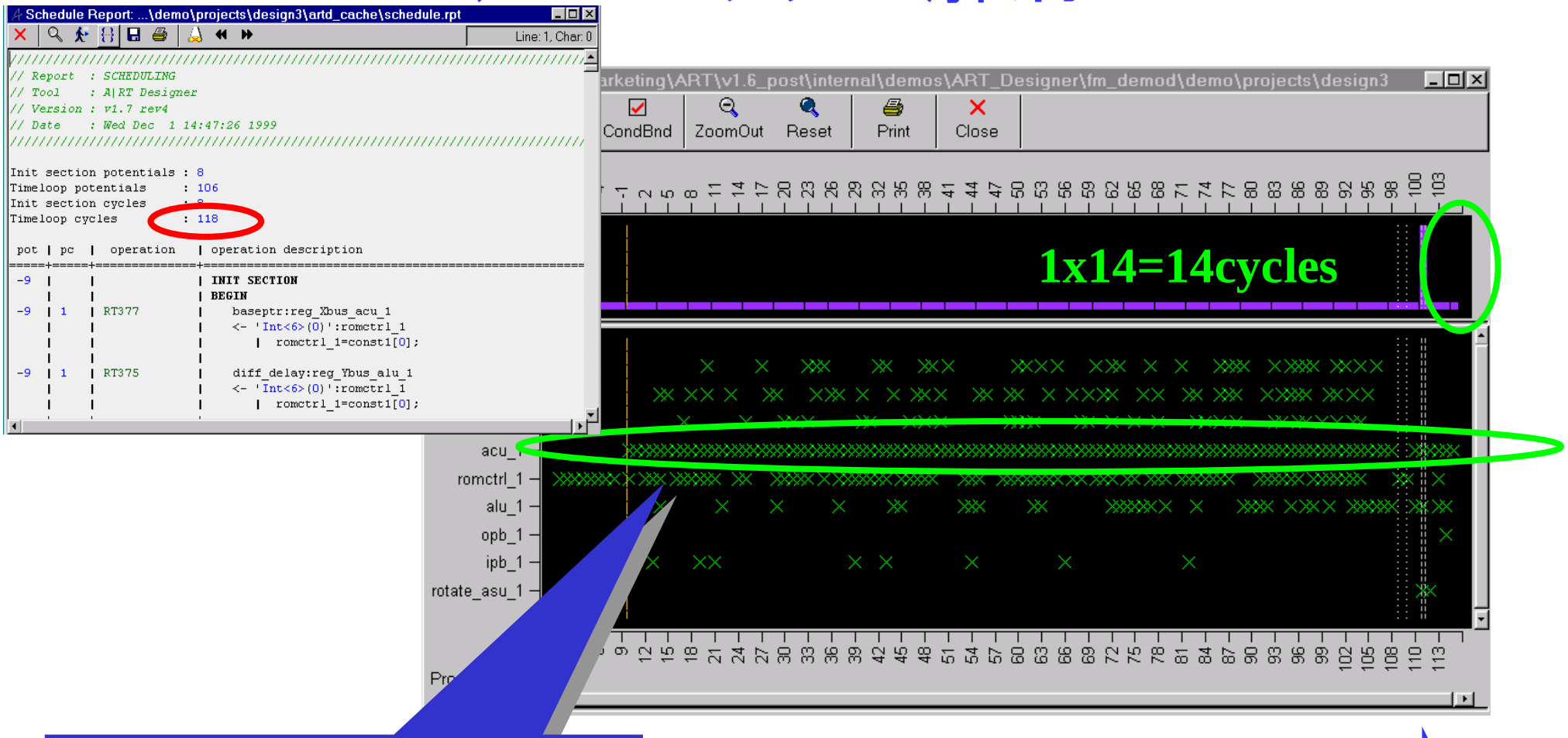
```
void rotate(
  cons . P_INDEX iter,
  P_FIX& xi,
  P_FIX& xq,
  P_FIX& xp)
{
#define BOOL Uint<1>

   BOOL xi_sign_bit,xq_sign_bit,different_sign;
   P_FIX angle,xi_inc,xq_inc;

   xi_inc = xq >> iter;
   xq_inc = xi >> iter;
   angle = lookup_angle_coeff[iter+1];

   xi_sign_bit = BOOL(xi < P_FIX(0));
   xq_sign_bit = BOOL(xq < P_FIX(0));
   different_sign = xi_sign_bit ^ xq_sign_bit;

   if (different_sign) {
      xi = xi+xi_inc;
      xq = xq-xq_inc;
      xp = xp+angle;
   } else {
      xi = xi-xi_inc;
      xq = xq+xq_inc;
      xp = xp-angle;
   }
}
```




```
assign_fcalltoasu("/.../*=rotate(*)","rotate_asu1");
```

Case Study

処理ネックの解消



Address Computation Bottleneck

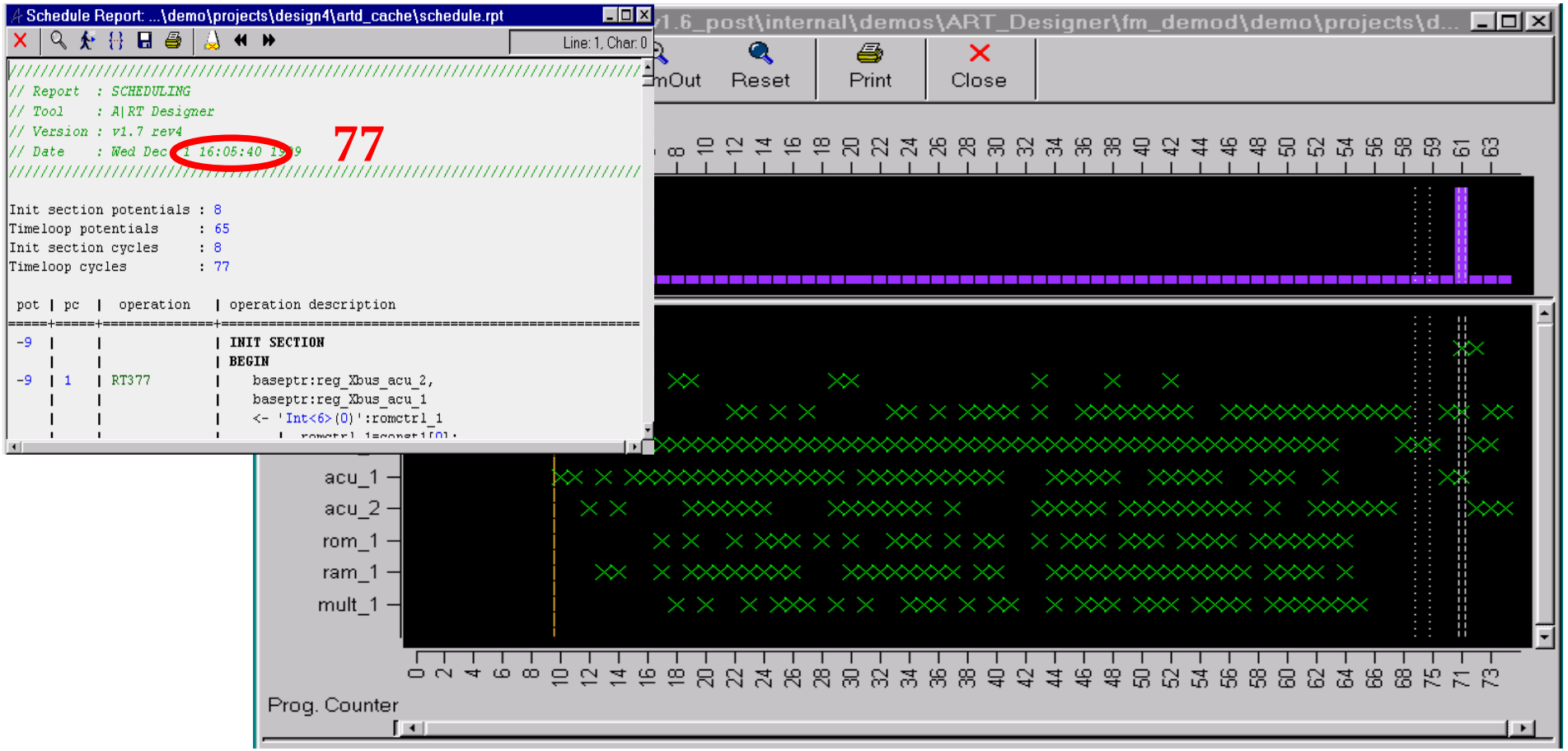
instantiate("acu_2”);

Frontier Design

Case Study

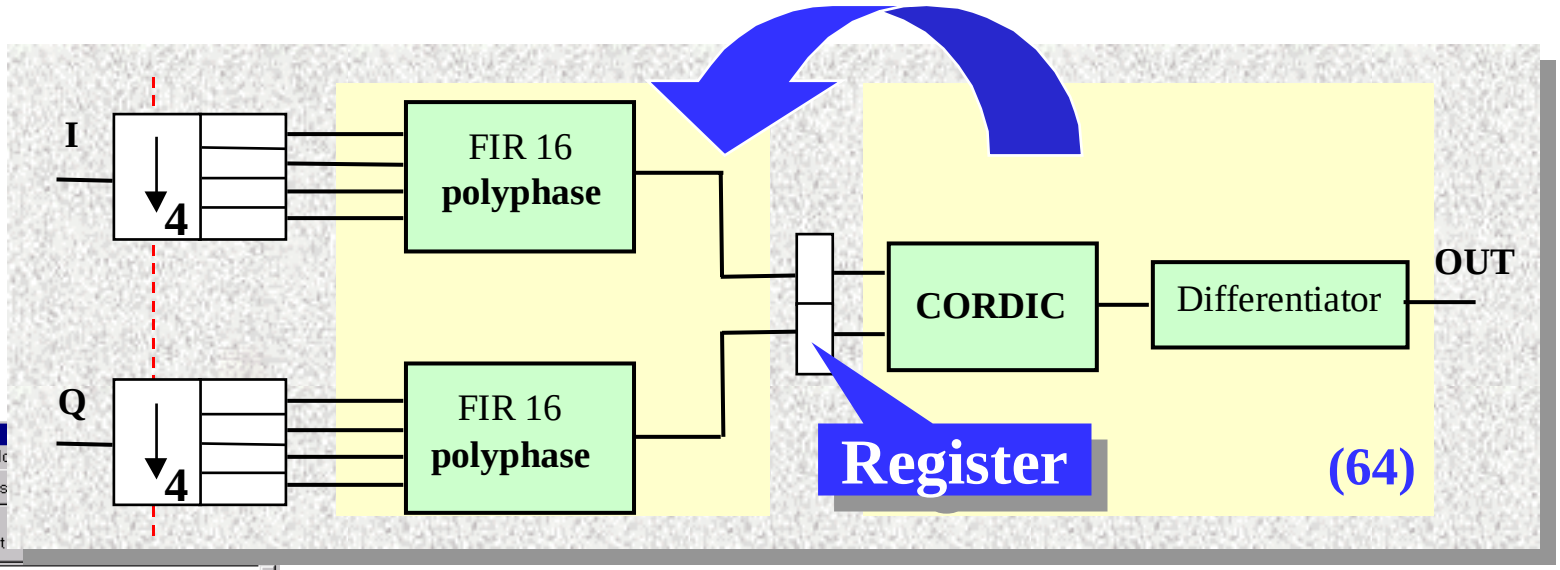
処理ネックの解消

-ACU_2の割当結果-



Case Study

パイプライン化



Edit/Compile Source

File Edit Search Options Reports Windo

File: P:\marketing\ART\v1.6_post\internal\demos

Import Save Edit Print Cut

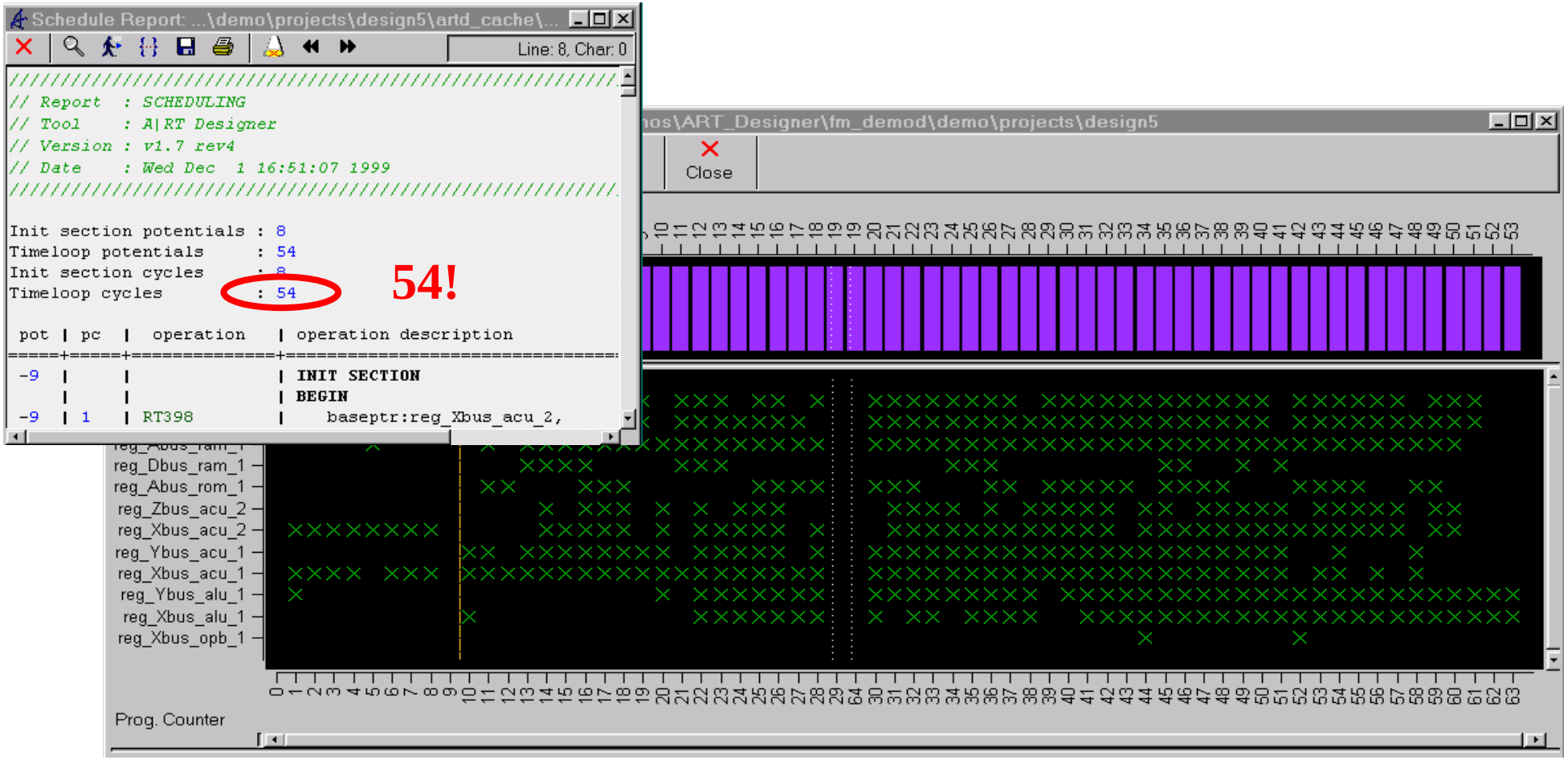
```
void fir_cordic(
   const P_FIX I_in[4],
   const P_FIX Q_in[4],
   P_FIX& Output)
{
#pragma OUT Output
  P_FIX Phase;
  static P_FIX I_out, Q_out;

   cordic(I_out, Q_out, Phase);
   Output=differentiator(Phase);
   // compute I and Q filters
   I_out = fir16<0>(I_in);
   Q_out = fir16<1>(Q_in);
   // compute angle
}
```

unroll("/.../cordic_loop");

Frontier Design

Case Study

パイプライン化の結果




```
Total number of fields and bits:
   datapath : 51 fields, 558 bits
   creg     : 1 fields, 1 bits
```

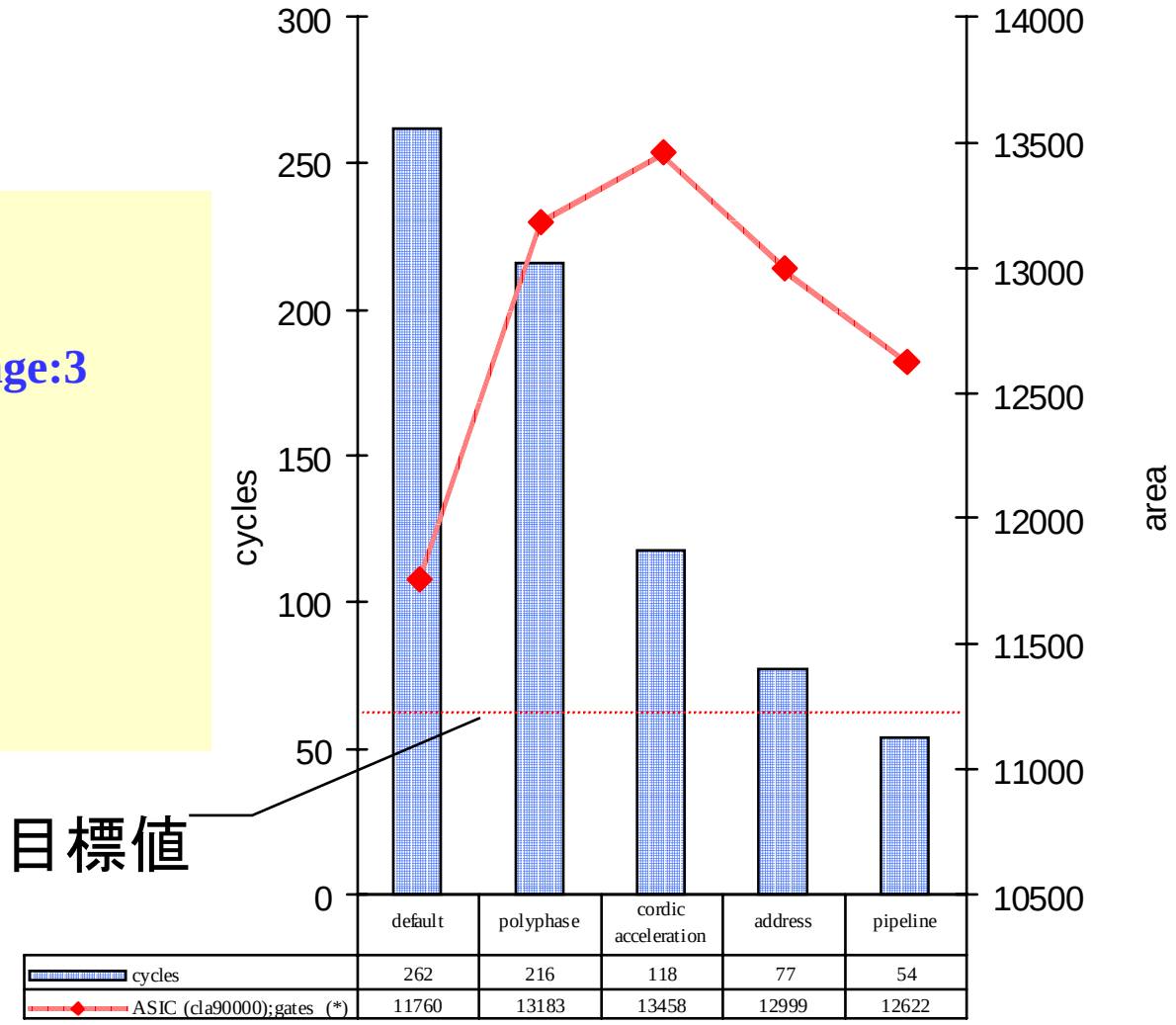

Frontier Design

Case study

結論

C-source:140
 # source code change:3
 # lines edited:4
 # hours spent:2

HDL-output:7750



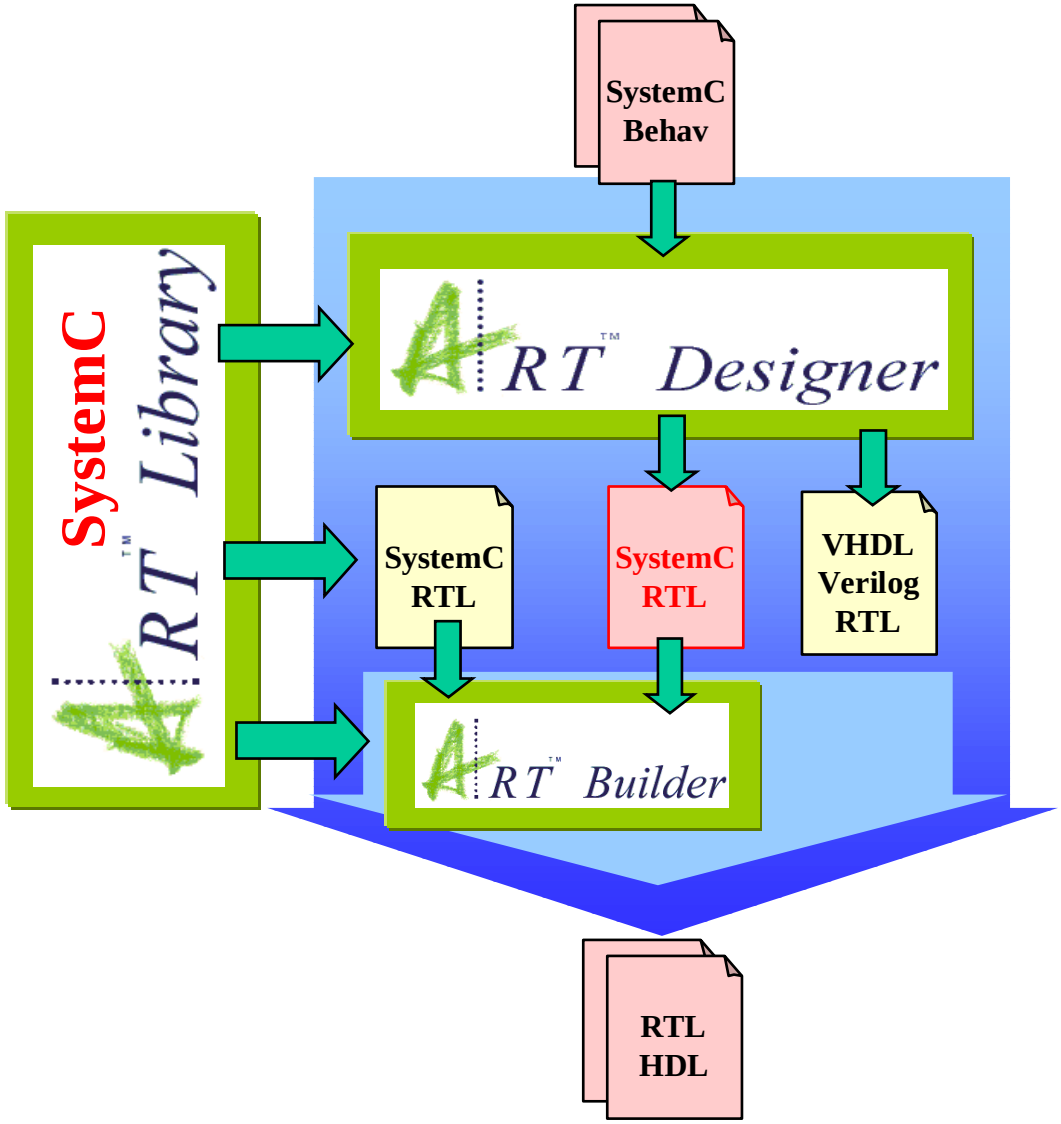
(*) excluding RAM, ROM

Frontierの A|RT と SystemC ?

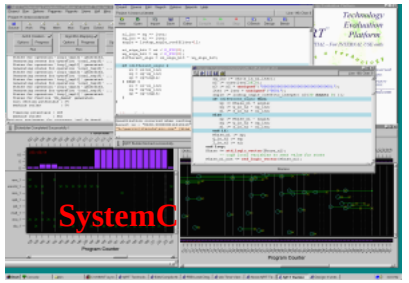
- **Frontier is co-developer of SystemC together with Synopsys and Coware**
  - **Frontier brings in the Fixed Point modeling library (ART Library)**
  - **Synopsys brings in the Scenery environment**
  - **Coware will provide its interprocess communication technology**
- **Frontier is focussing on providing synthesis solutions based on SystemC**
  - **ART Builder : RTL-C to RTL-HDL**
  - **ART Designer : Behav-C to RTL-HDL**

Frontier Design

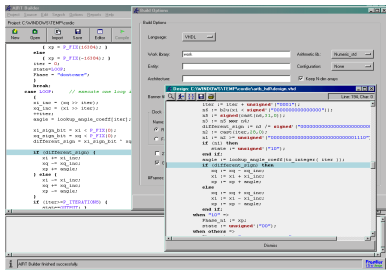
A|RT と SystemC



System Design

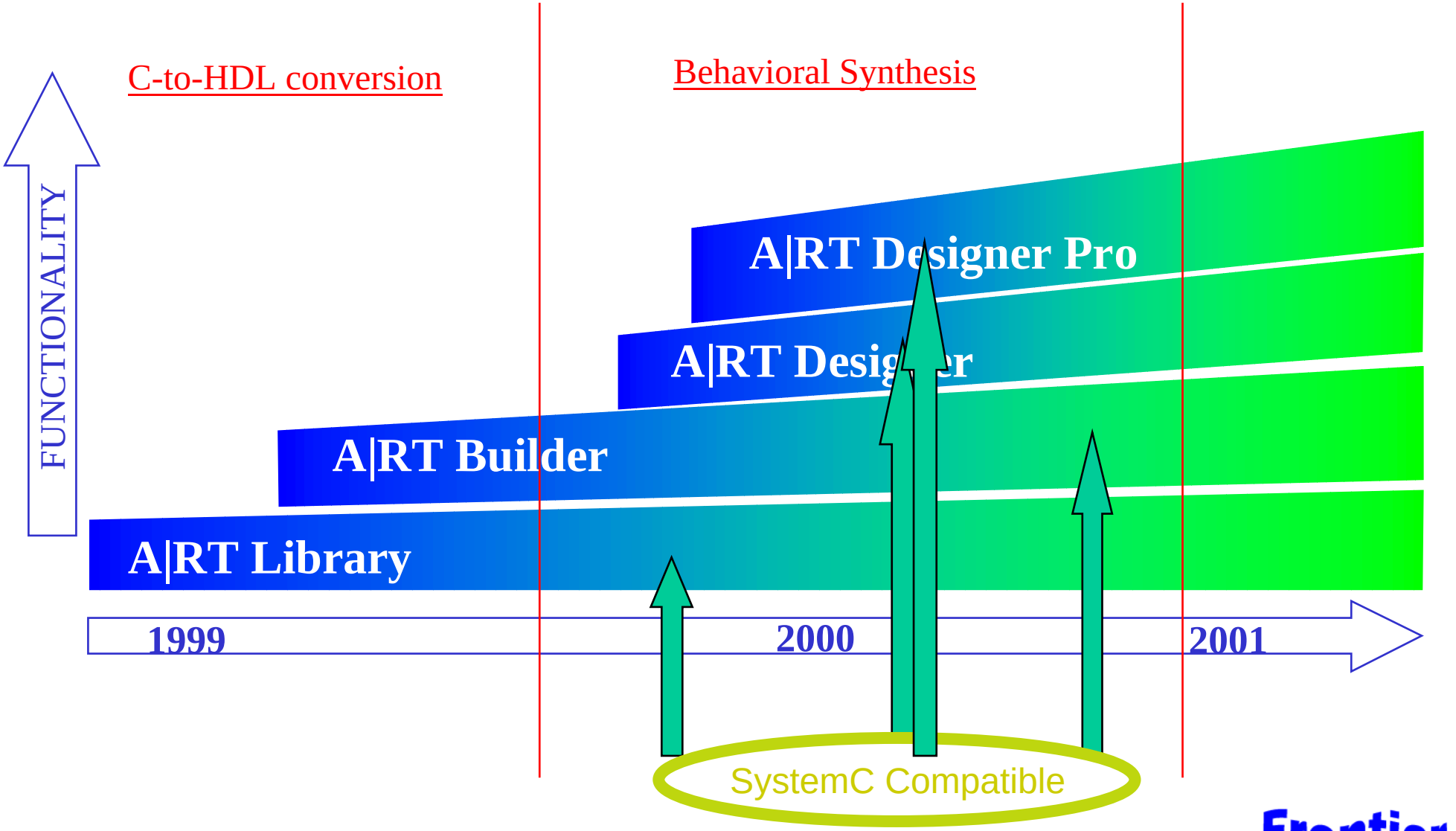


RTL Design



Frontier Design

製品ロードマップ


C-to-HDL conversion
Behavioral Synthesis
FUNCTIONALITY
A|RT Designer Pro
A|RT Designer
A|RT Builder
A|RT Library
1999
2000
2001
SystemC Compatible

まとめ

- **Frontier社はC言語からの設計、アーキテクチャ合成ツールのリーダーです。**
  - **ART Library : C based hardware modeling**
  - **ART Builder : “RTL-C to RTL-HDL” translation**
  - **ART Designer : “Behav-C to RTL-HDL” synthesis**
- **Frontier社は従来のVHDL/Verilog設計の上流設計フローとして、C言語での設計手法を提案しております。**
- **Frontier社は SystemC standardに準拠した設計ツールの開発を推進しております**