

RX Family

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Simple I²C Module Using Firmware Integration Technology

Introduction

This application note describes the simple I²C module using firmware integration technology (FIT) for communications between devices using the serial communications interface (SCI).

Target Device

This API supports the following device.

- RX111 Group
- RX110 Group
- RX113 Group
- RX64M Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Related Documents

- Firmware Integration Technology User's Manual (R01AN1833EU)
- Board Support Package Module Using Firmware Integration Technology (R01AN1685EU)
- Adding Firmware Integration Technology Modules to Projects (R01AN1723EU)
- Adding Firmware Integration Technology Modules to CubeSuite+ Projects (R01AN1826EJ)

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1. Overview

The simple I²C module using firmware integration technology (SCI simple I²C mode FIT module ⁽¹⁾) provides a method to transmit and receive data between the master and slave devices using the SCI. The SCI simple I²C mode is in compliance with single master mode of the NXP I²C-bus (Inter-IC-Bus) interface.

Note:

1. When the description says “module” in this document, it indicates the SCI simple I²C mode FIT module.

Features supported by this module are as follows:

- Single master mode (slave transmission or slave reception is not supported).
- Circuit to generate waveforms for conditions.
- Communication mode can be standard or fast mode and the maximum communication rate is 384 kbps.

Limitations

- This module cannot be used with the DTC.
- This module does not support transmission with 10-bit address.
- Multiple interrupts are not supported.
- API function calls except for the R_SCI_IIC_GetStatus function are disabled in the callback function.
- The I flag must be set to 1 to use interrupts.

1.1 SCI Simple I²C Mode FIT Module

This module is implemented in a project and used as the API. Refer to 2.9 Adding the FIT Module to Your Project for details on implementing the module to the project.

1.2 Outline of the API

Table 1.1 lists the API Functions and Table 1.2 lists the Required Memory Size.

Table 1.1 API Functions

Item	Contents
R_SCI_IIC_Open()	Initializes the SCI to prepare for this module.
R_SCI_IIC_MasterSend()	Starts master transmission. Changes the transmit pattern according to the parameters. Operates batched processing until stop condition generation.
R_SCI_IIC_MasterReceive()	Starts master reception. Changes the receive pattern according to the parameters. Operates batched processing until stop condition generation.
R_SCI_IIC_Close()	Releases channels associated with the SCI.
R_SCI_IIC_GetStatus()	Used to verify the SCI state.
R_SCI_IIC_Control()	Performs processing such as an internal initialization mainly when a communication error occurs.
R_SCI_IIC_GetVersion()	Returns the module version.

Table 1.2 Required Memory Size

Memory Used	Size	Remarks
ROM	4518 bytes	
RAM	41 bytes	
Maximum user stack usage	148 bytes	
Maximum interrupt stack usage	152 bytes	

* The table lists values when the default values are set to the compile options and the RX111 Group is used. The required memory size varies depending on the C compiler version and compile options.

1.3 Overview of SCI Simple I²C Mode FIT Module

1.3.1 Specifications of SCI Simple I²C Mode FIT Module

- This module supports master transmission and reception.
 - There are four transmit patterns that can be used for master transmission. Refer to 1.3.2 for details on master transmission.
 - Master reception and master composite can be selected for master reception. Refer to 1.3.3 for details on master reception.
- An interrupt occurs when any of the following operations completes: start condition generation, slave address transmission, data reception, or stop condition generation. In the simple I²C interrupt handling, the communication control function is called and the operation is continued.
- The module supports multiple channels. When the device used has multiple channels, simultaneous communication is available using multiple channels.
- Multiple slave devices on the same channel bus can be controlled. However, while communication is in progress (the period from start condition generation to stop condition generation), communication with other devices is not available. Figure 1.1 shows an Example of Controlling Multiple Slave Devices.

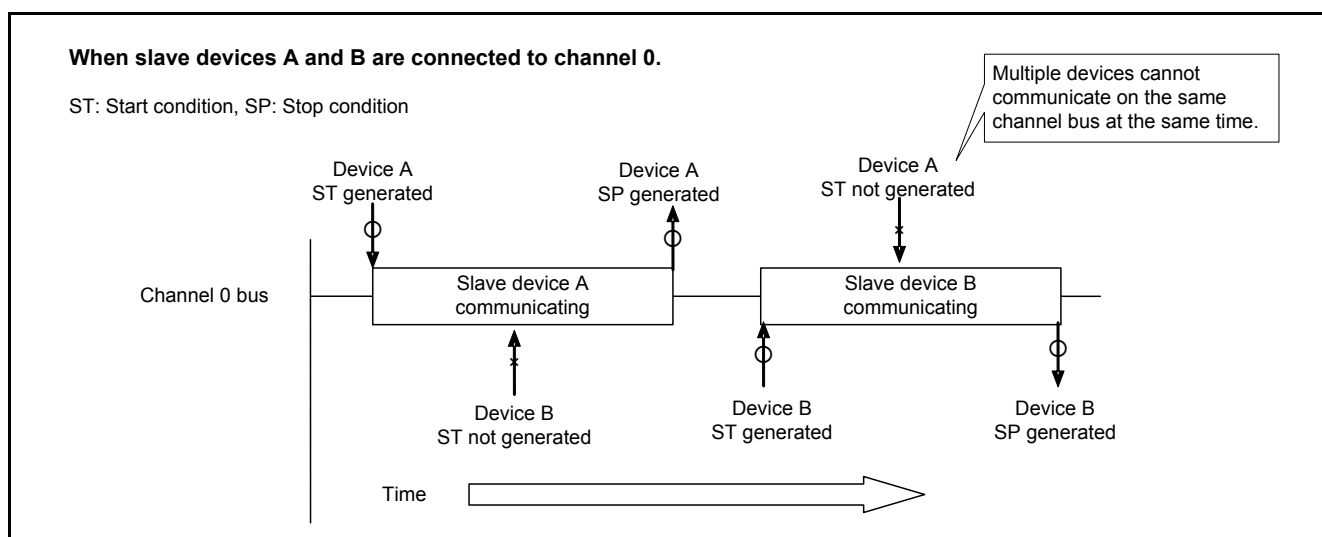


Figure 1.1 Example of Controlling Multiple Slave Devices

1.3.2 Master Transmission

Data is transmitted from the master device (master (RX MCU)) to the slave device (slave).

With this module, four patterns of waveforms can be generated for master transmission. A pattern is selected according to the arguments set in the parameters which are members of the I²C communication information structure. Refer to 2.7 Parameters for details on the I²C communication information structure. Figure 1.2 to Figure 1.5 show the transmit patterns.

(1) Pattern 1

Data is transmitted from the master (RX MCU) to the slave.

A start condition is generated and then the slave address is transmitted. The eighth bit specifies the transfer direction. This bit is set to 0 (write) when transmitting. Then the first data is transmitted. The first data is used when there is data to be transmitted in advance before performing the data transmission. For example, if the slave is an EEPROM, the EEPROM internal address can be transmitted. Next the second data is transmitted. The second data is the data to be written to the slave. When a data transmission has started and all data transmissions have completed, a stop condition is generated, and the bus is released.

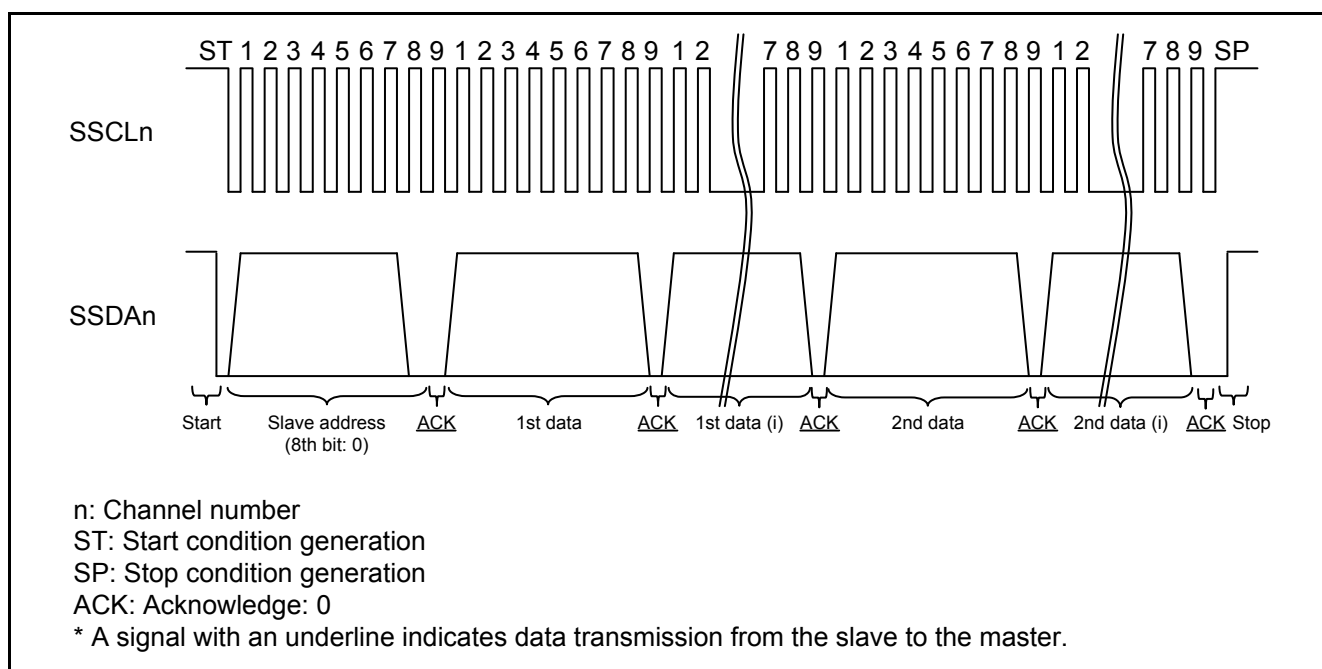


Figure 1.2 Signals for Pattern 1 of Master Transmission

(2) Pattern 2

Data is transmitted from the master (RX MCU) to the slave. However, when the first data is not set, transmission for the first data is not performed.

Operations from start condition generation through to slave address transmission are the same as the operations for pattern 1. Then the second data is transmitted without transmitting the first data. When all data transmissions have completed, a stop condition is generated and the bus is released.

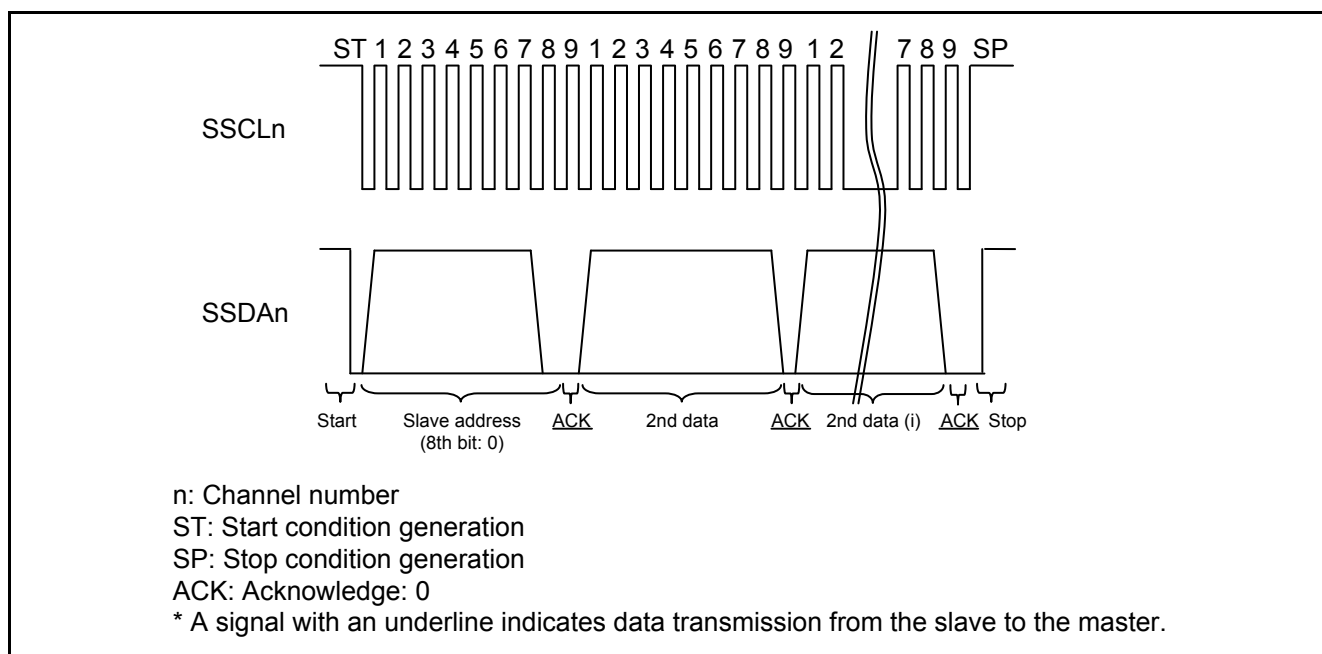


Figure 1.3 Signals for Pattern 2 of Master Transmission

(3) Pattern 3

Operations from start condition generation through to slave address transmission are the same as the operations for pattern 1. When neither the first data nor the second data are set, data transmission is not performed, then a stop condition is generated, and the bus is released.

This pattern is useful for detecting connected devices or when performing acknowledge polling to verify the EEPROM rewriting state.

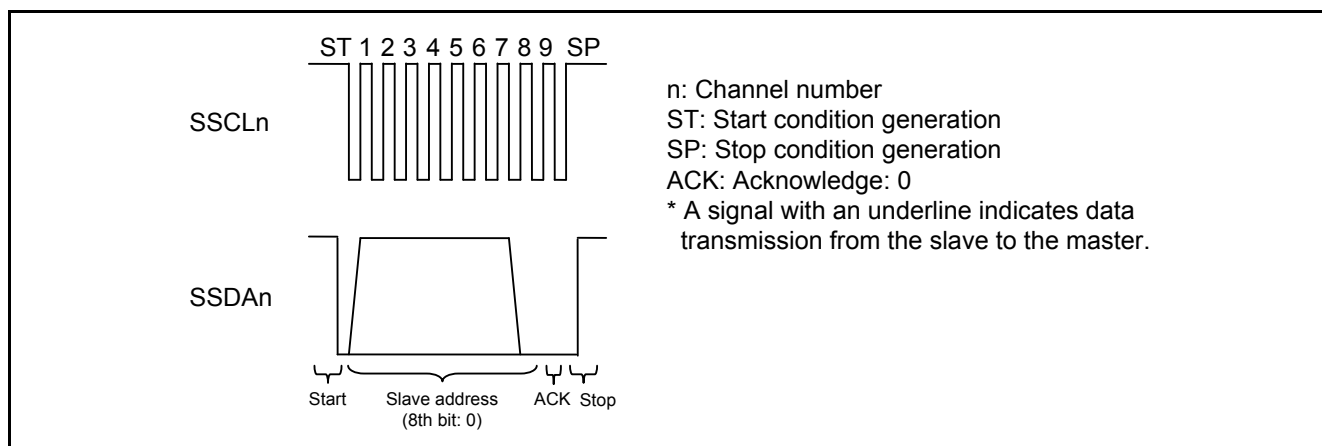


Figure 1.4 Signals for Pattern 3 of Master Transmission

(4) Pattern 4

After a start condition is generated, when the slave address, first data, and second data are not set, slave address transmission and data transmission are not performed. Then a stop condition is generated and the bus is released.

This pattern is useful for just releasing the bus.

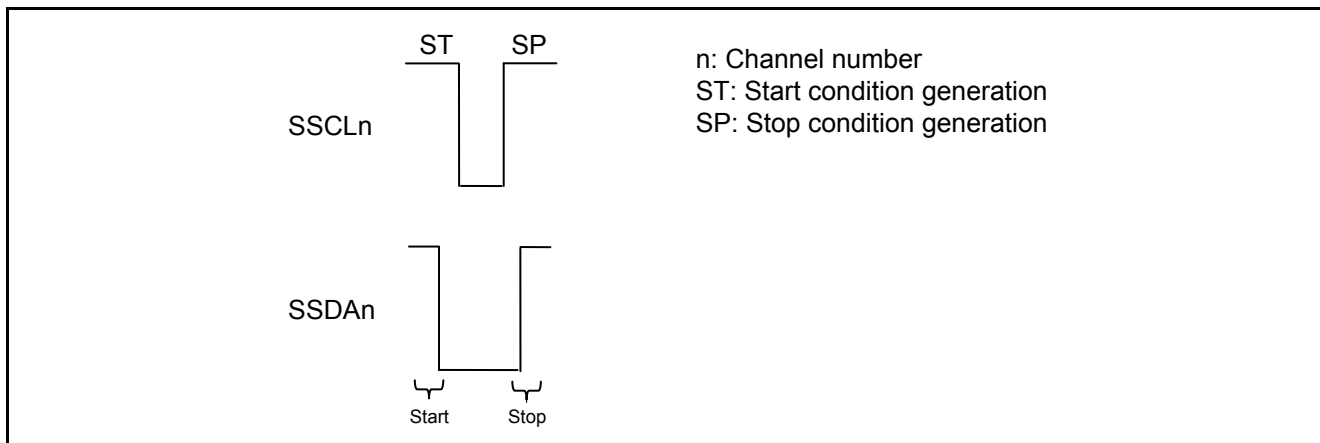


Figure 1.5 Signals for Pattern 4 of Master Transmission

Figure 1.6 shows the procedure of master transmission. The callback function is called after generating a stop condition. Specify the function name in the CallBackFunc of the I²C communication information structure member.

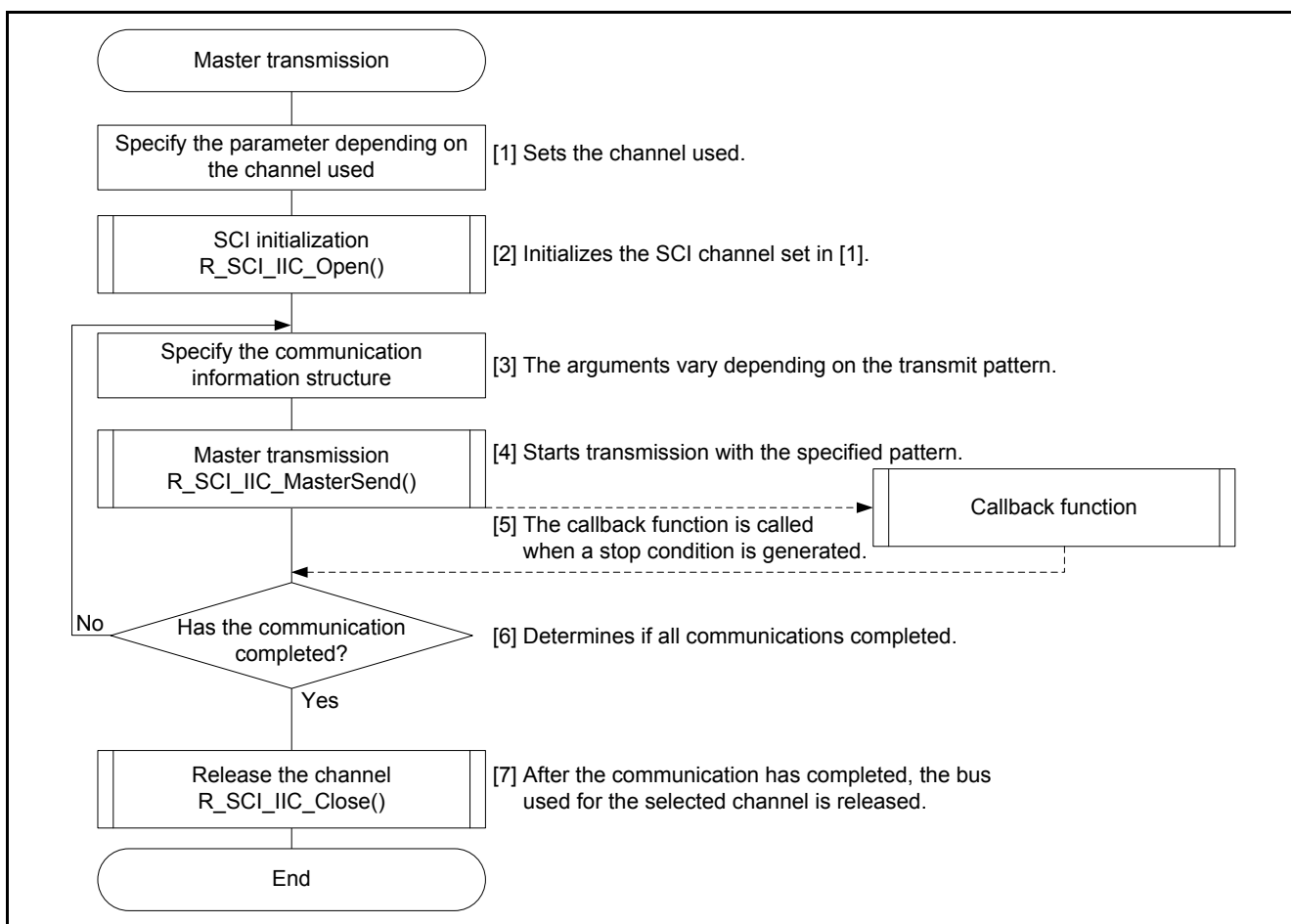


Figure 1.6 Example of Master Transmission

1.3.3 Master Reception

The master (RX MCU) receives data from the slave. This module supports master reception and master composite. The receive pattern is selected according to the arguments set in the parameters which are members of the I²C communication information structure. Refer to 2.7 Parameters for details on the I²C communication information structure. Figure 1.7 and Figure 1.8 show receive patterns.

(1) Master Reception

The master (RX MCU) receives data from the slave.

A start condition is generated and then the slave address is transmitted. The eighth bit specifies the transfer direction. This bit is set to 1 (read) when receiving. Then data reception starts. An ACK is transmitted each time 1-byte data is received except the last data. A NACK is transmitted when the last data is received to notify the slave that all data receptions have completed. Then a stop condition is generated and the bus is released.

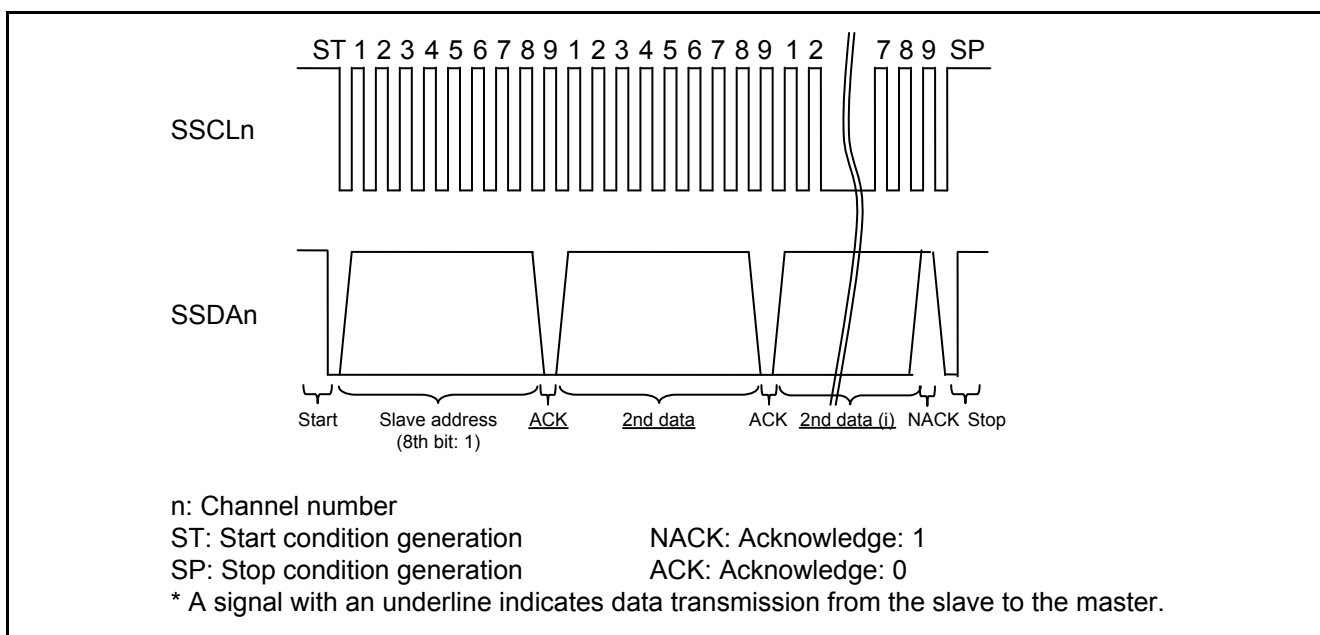


Figure 1.7 Signals for Master Reception

(2) Master Composite

The master (RX MCU) transmits data to the slave (master transmission). After the transmission completes, a restart condition is generated, the transfer direction is changed to 1 (read), and the master receives data from the slave (master reception).

A start condition is generated and then the slave address is transmitted. The eighth bit is the bit specifies the transfer direction. This bit is set to 0 (write) when transmitting. Then the first data is transmitted. When the data transmission completes, a restart condition is generated and the slave address is transmitted. Then the eighth bit is set to 1 (read) and a data reception starts. An ACK is transmitted each time 1-byte data is received except the last data. A NACK is transmitted when the last data is received to notify the slave that all data receptions have completed. Then a stop condition is generated and the bus is released.

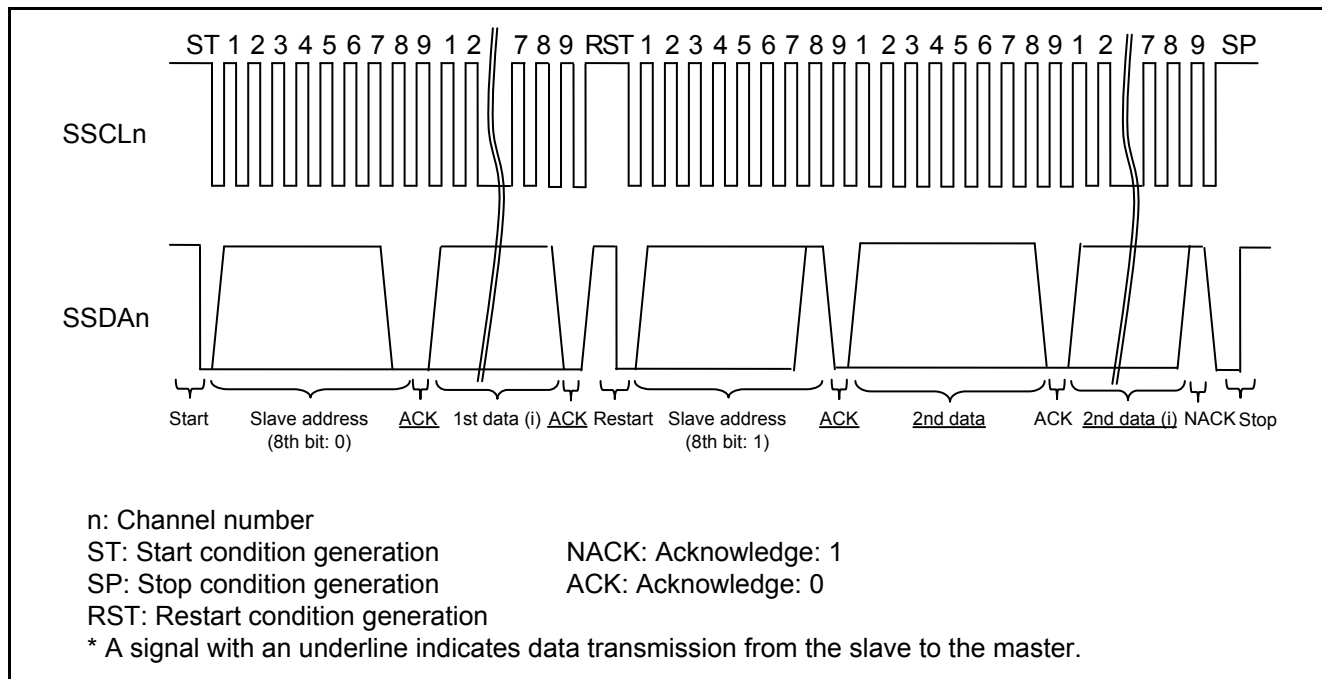


Figure 1.8 Signals for Master Composite

Figure 1.9 shows the procedure of master reception. The callback function is called after generating a stop condition. Specify the function name in the CallBackFunc of the I²C communication information structure member.

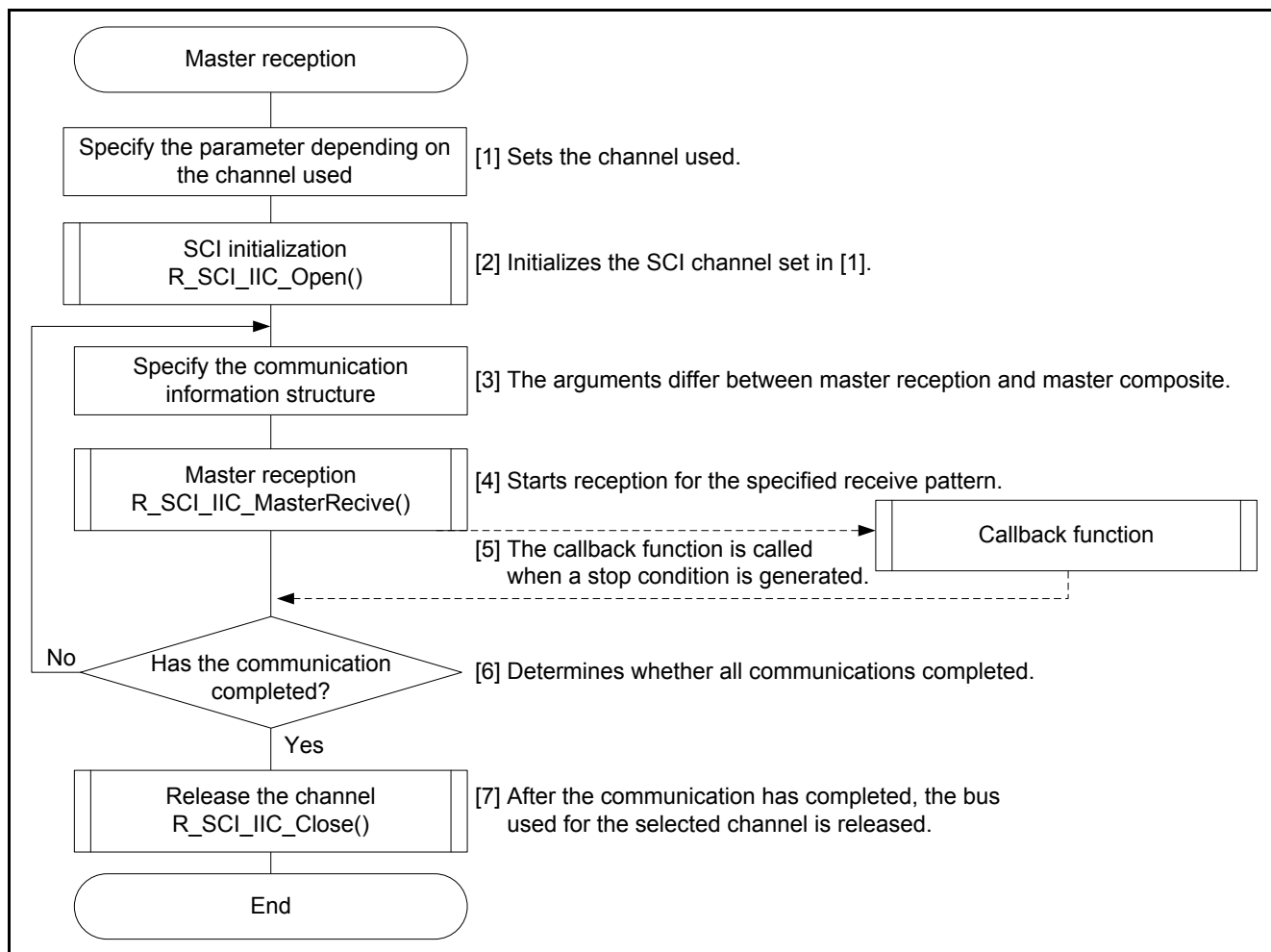


Figure 1.9 Example of Master Reception

1.3.4 State Transition

States entered in this module are uninitialized state, idle state, and communicating state.

Figure 1.10 shows the State Transition Diagram.

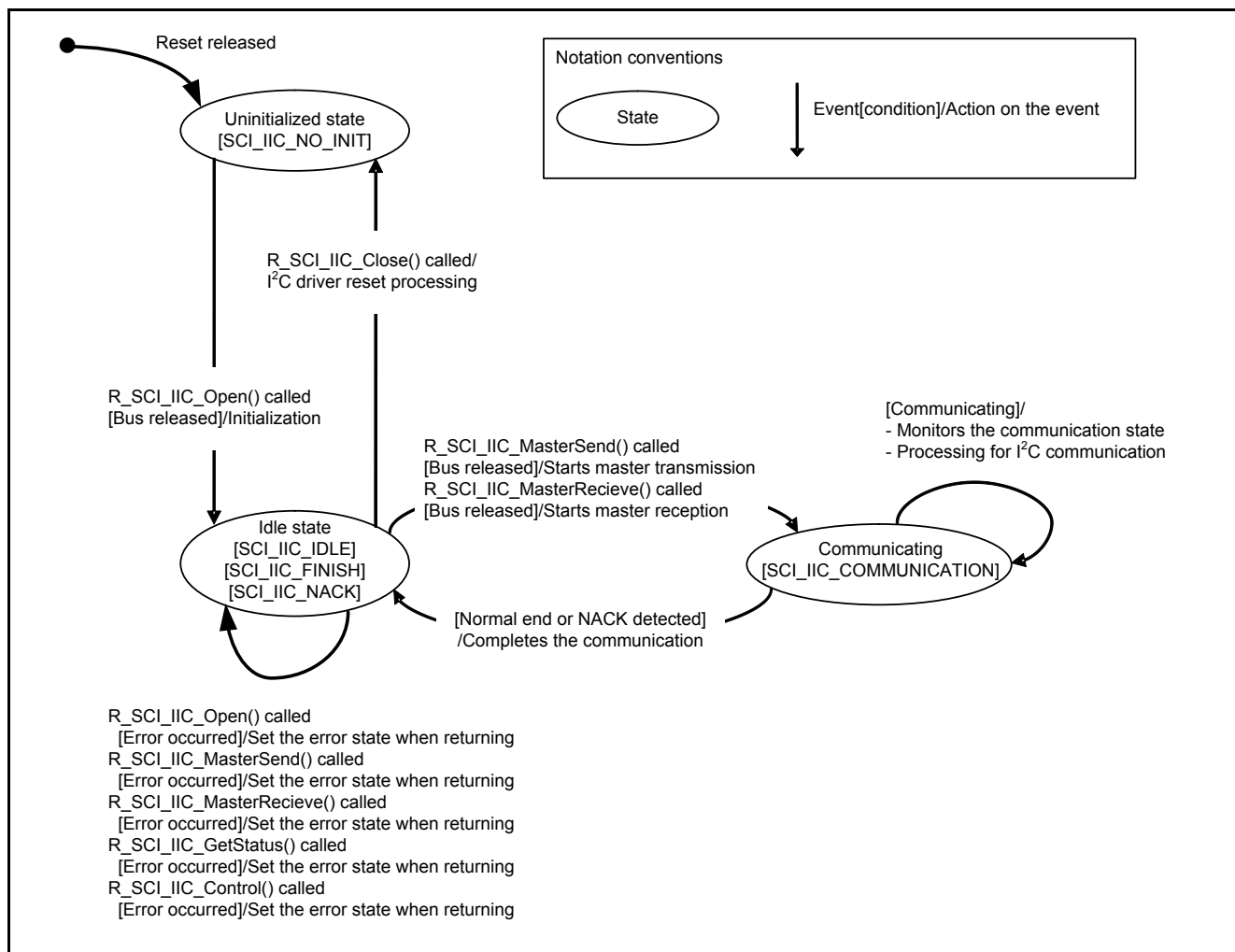


Figure 1.10 State Transition Diagram

1.3.5 Flags when Transitioning States

dev_sts is the device state flag and is one of the I²C communication information structure members. The flag stores the communication state of the device. Using this flag enables controlling multiple slaves on the same channel.

Table 1.3 lists the Device State Flags when Transitioning States.

Table 1.3 Device State Flags when Transitioning States

State	Device State Flag (dev_sts)
Uninitialized state	SCI_IIC_NO_INIT
Idle states	SCI_IIC_IDLE SCI_IIC_FINISH SCI_IIC_NACK
Communicating (master transmission)	SCI_IIC_COMMUNICATION
Communicating (master reception)	SCI_IIC_COMMUNICATION
Communicating (master composite)	SCI_IIC_COMMUNICATION
Error	SCI_IIC_ERROR

2. API Information

This driver API adheres to the Renesas API naming standards.

2.1 Hardware Requirements

This driver requires your MCU supports the following feature:

- SCI

2.2 Software Requirements

This driver is dependent upon the following packages:

- r_bsp

2.3 Supported Toolchains

This driver is tested and works with the following toolchain:

- Renesas RX Toolchain v.2.01

2.4 Header Files

All API calls and their supporting interface definitions are located in `r_sci_iic_rx_if.h`.

2.5 Integer Types

This project uses ANSI C99. These types are defined in `stdint.h`.

2.6 Configuration Overview

The configuration options in this module are specified in `r_sci_iic_rx_config.h`. The option names and setting values are listed in the table below.

Configuration options in <i>r_sci_iic_rx_config.h</i> (1/3)	
<pre>#define SCI_IIC_CFG_PARAM_CHECKING_ENABLE - Default value = 1</pre>	Selectable whether to include parameter checking in the code. - When this is set to 0, parameter checking is omitted. - When this is set to 1, parameter checking is included.
<pre>#define SCI_IIC_CFG_CHi_INCLUDED i = 0 to 9, 12 - When i = 1, the default value = 1 - When i = 0, 2 to 9, or 12, the default value = 0</pre>	Selectable whether to use available channels. - When this is set to 0, relevant processes for the channel are omitted from the code. - When this is set to 1, relevant processes for the channel are included in the code.
<pre>#define SCI_IIC_CFG_CHi_BITRATE_BPS i = 0 to 9, 12 - Default value = 384000 for all</pre>	Specifies the bit rate. Specify a value less than or equal to 384000 (384 kbit/sec.).
<pre>#define SCI_IIC_CFG_CHi_INT_PRIORITY i = 0 to 9, 12 - Default value = 2 for all</pre>	Specifies interrupt priority levels for condition generation, receive-data-full, transmit-data-empty, and transmit-end interrupts. Specify the level between 1 and 15.
<pre>#define SCI_IIC_CFG_CHi_DIGITAL_FILTER i = 0 to 9, 12 - Default value = 1 for all</pre>	Selectable whether to use the noise cancellation function for the SSCL and SSDA input signals. - When this is set to 0, the noise cancellation function is disabled. - When this is set to 1, the noise cancellation function is enabled.
<pre>#define SCI_IIC_CFG_CHi_FILTER_CLOCK i = 0 to 9, 12 - Default value = 1 for all</pre>	Select the sampling clock used for digital noise filter. - When this is set to 1, the clock divided by 1 is used. - When this is set to 2, the clock divided by 2 is used. - When this is set to 3, the clock divided by 4 is used. - When this is set to 4, the clock divided by 8 is used.
<pre>#define SCI_IIC_CFG_CHi_SSDA_DELAY_SELECT i = 0 to 9, 12 - Default value = 1 for all</pre>	Select the delay time of the SSDA pin output to the falling on the SSCL pin. Specify the delay between 1 and 31.

Configuration options in *r_sci_iic_rx_config.h* (2/3)

<pre>#define SCI_IIC_CFG_BUS_CHECK_COUNTER i = 0 to 9, 12 - Default value = 1000</pre>	<p>Specifies the timeout counter (number of times to perform bus checking) when the simple I²C API function performs bus checking. Specify a value less than or equal to 0xFFFFFFFF.</p> <p>The bus checking is performed after generating each condition using the simple I²C control function (R_SCI_IIC_Control function).</p> <p>With the bus checking, the timeout counter is decremented after generating each condition. When the counter reaches 0, the API determines that a timeout has occurred and returns an error (Busy) as the return value.</p> <p>* The timeout counter is used for the bus not to be locked by the bus lock or others. Therefore specify the value greater than or equal to the time for that the other device holds the SCL pin low.</p> <p>Setting time for the timeout (ns) $\approx (\frac{1}{f_{CLK}} \text{ (Hz)}) \times \text{counter value} \times 10$</p>
<pre>#define SCI_IIC_CFG_PORT_SETTING_PROCESSING - Default value = 1</pre>	<p>Specifies whether to include processing for port setting ^(*) in the code.</p> <p>* Processing for port setting is the setting to use ports selected by SCI_IIC_CFG_CHi_SSCL_GP, SCI_IIC_CFG_CHi_SSCL_PIN, SCI_IIC_CFG_CHi_SSDA_GP, and SCI_IIC_CFG_CHi_SSDA_PIN as pins SSCL and SSDA.</p> <ul style="list-style-type: none"> - When this is set to 0, processing for port setting is omitted from the code. - When this is set to 1, processing for port setting is included in the code.

Configuration options in *r_sci_iic_rx_config.h* (3/3)

<pre>#define SCI_IIC_CFG_CHi_SSCL_GP i = 0 to 9, 12 - When i = 0, the default value = "PORT2_GR" - When i = 1, the default value = "PORT1_GR" - When i = 2, the default value = "PORT5_GR" - When i = 3, the default value = "PORT2_GR" - When i = 4, the default value = "PORTB_GR" - When i = 5, the default value = "PORTC_GR" - When i = 6, the default value = "PORTB_GR" - When i = 7, the default value = "PORT9_GR" - When i = 8, the default value = "PORTC_GR" - When i = 9, the default value = "PORTB_GR" - When i = 12, the default value = "PORTE_GR"</pre>	<p>Selects port groups used as the SSCL pins. Specify the value from "PORT0_GR" to "PORTJ_GR".</p>
<pre>#define SCI_IIC_CFG_CHi_SSCL_PIN i = 0 to 9, 12 - When i = 0, the default value = 1 - When i = 1, the default value = 5 - When i = 2, the default value = 2 - When i = 3, the default value = 5 - When i = 4, the default value = 0 - When i = 5, the default value = 2 - When i = 6, the default value = 0 - When i = 7, the default value = 2 - When i = 8, the default value = 6 - When i = 9, the default value = 6 - When i = 12, the default value = 2</pre>	<p>Selects pins used as the SSCL pins. Specify the value from 0 to 7.</p>
<pre>#define SCI_IIC_CFG_CHi_SSDA_GP i = 0 to 9, 12 - When i = 0, the default value = "PORT2_GR" - When i = 1, the default value = "PORT1_GR" - When i = 2, the default value = "PORT5_GR" - When i = 3, the default value = "PORT2_GR" - When i = 4, the default value = "PORTB_GR" - When i = 5, the default value = "PORTC_GR" - When i = 6, the default value = "PORTB_GR" - When i = 7, the default value = "PORT9_GR" - When i = 8, the default value = "PORTC_GR" - When i = 9, the default value = "PORTB_GR" - When i = 12, the default value = "PORTE_GR"</pre>	<p>Selects port groups used as the SSDA pin. Specify the value from "PORT0_GR" to "PORTJ_GR".</p>
<pre>#define SCI_IIC_CFG_CHi_SSDA_PIN i = 0 to 9, 12 - When i = 0, the default value = 0 - When i = 1, the default value = 6 - When i = 2, the default value = 0 - When i = 3, the default value = 3 - When i = 4, the default value = 1 - When i = 5, the default value = 3 - When i = 6, the default value = 1 - When i = 7, the default value = 0 - When i = 8, the default value = 7 - When i = 9, the default value = 7 - When i = 12, the default value = 1</pre>	<p>Selects port groups used as the SSDA pin. Specify the value from 0 to 7.</p>

2.7 Parameters

This section describes the structure whose members are API parameters. This structure is located in `r_sci_iic_rx_if.h` as are the prototype declarations of API functions.

```
typedef struct
{
    uint8_t rsv2; /* Reserved area */
    uint8_t rsv1; /* Reserved area */
    sci_iic_ch_dev_status_t dev_sts; /* Device state flag */
    uint8_t ch_no; /* Channel number for the device used */
    sci_iic_callback callbackfunc; /* Callback function */
    uint32_t cnt2nd; /* Second data counter (number of bytes) */
    uint32_t cnt1st; /* First data counter (number of bytes) */
    uint8_t * p_data2nd; /* Pointer to the buffer to store the second data */
    uint8_t * p_data1st; /* Pointer to the buffer to store the first data */
    uint8_t * p_slv_addr; /* Pointer to the buffer to store the slave address */
} sci_iic_info_t;
```

2.8 Return Values

This section describes return values of API functions. This enumeration is located in `r_sci_iic_rx_if.h` as are the prototype declarations of API functions.

```
typedef enum /* Simple I2C-bus API state codes */
{
    SCI_IIC_SUCCESS, /* Processing completed successfully */
    SCI_IIC_ERR_LOCK_FUNC, /* Multiple calls occurred on the same channel. */
    SCI_IIC_ERR_INVALID_CHAN, /* Nonexistent channel */
    SCI_IIC_ERR_INVALID_ARG, /* Invalid parameter */
    SCI_IIC_ERR_NO_INIT, /* Uninitialized state */
    SCI_IIC_ERR_BUS_BUSY, /* Bus is busy. This state occurs with the following cases: */
                        /* The initialization function or a start function is */
                        /* called during communication. */
                        /* A start function or advance function is called while */
                        /* another device on the same channel is communicating. */
    SCI_IIC_ERR_OTHER /* Other error */
} sci_iic_return_t;
```

2.9 Adding the FIT Module to Your Project

The module must be added to an existing e2Studio project.

It is best to use the e2Studio FIT plug-in to add the FIT module to your project as that will automatically update the include file paths for you. To add the FIT module using the plug-in, refer to “2. Adding FIT Modules to e2 studio Projects Using FIT Plug-In” in the application note “Adding Firmware Integration Technology Modules to Projects (R01AN1723EU)”.

Alternatively, the FIT module can be added manually. To add the FIT module manually, refer to “3. Adding FIT Modules to e2 studio Projects Manually” in the application note “Adding Firmware Integration Technology Modules to Projects (R01AN1723EU)”.

When using the FIT module, the BSP FIT module also needs to be added to the project. For details on the BSP FIT module, refer to the application note “Board Support Package Module Using Firmware Integration Technology (R01AN1685EU)”.

3. API Functions

3.1 R_SCI_IIC_Open()

This function is required first when using the simple I²C API.

Format

```
sci_iic_return_t R_SCI_IIC_Open(  
    sci_iic_info_t * p_sci_iic_info /* Structure data */  
)
```

Parameters

** p_sci_iic_info*

This is the pointer to the I²C communication information structure.

Only the member of the structure used in this function is described here. Refer to 2.7 Parameters for details on the structure.

For the parameter which has ‘(to be updated)’ in the comment below, the argument for the parameter will be updated during the API execution.

```
sci_iic_ch_dev_status_t dev_sts; /* Device state flag (to be updated) */  
uint8_t ch_no; /* Channel number */
```

Return Values

SCI_IIC_SUCCESS /* Processing completed successfully */

SCI_IIC_ERR_LOCK_FUNC /* The API is locked by the other task. */

SCI_IIC_ERR_INVALID_CHAN /* Nonexistent channel */

SCI_IIC_ERR_INVALID_ARG /* Invalid parameter */

SCI_IIC_ERR_OTHER /* The event occurred is invalid in the current state. */

Properties

Prototyped in r_sci_iic_rx_if.h.

Description

Performs the initialization to start the simple I²C-bus communication. Sets the SCI channel specified by the parameter. If the state of the channel is ‘uninitialized (SCI_IIC_NO_INIT)’, the following processes are performed.

- Setting the state flag
- Setting I/O ports
- Allocating I²C output ports
- Cancelling SCI module-stop state
- Initializing variables used by the API
- Initializing the SCI registers used for the simple I²C-bus communication
- Disabling the SCI interrupt

Reentrant

Function is reentrant for different channels.

Example

```
volatile sci_iic_return_t ret;  
sci_iic_info_t      siic_info;  
  
siic_info.dev_sts = 0;  
siic_info.ch_no = 1;  
  
ret = R_SCI_IIC_Open(&siic_info);
```

Special Notes

None

3.2 R_SCI_IIC_MasterSend()

This function is used when the master transmission starts.

Format

```
sci_iic_return_t R_SCI_IIC_MasterSend(
    sci_iic_info_t * p_sci_iic_info /* Structure data */
)
```

Parameters

**p_sci_iic_info*

This is the pointer to the I²C communication information structure. The transmit patterns can be selected from four patterns by the parameter. Refer to the Special Notes in this section for available settings and the setting values for each transmit pattern. Also refer to 1.3.2 Master Transmission for details of each pattern.

Only members of the structure used in this function are described here. Refer to 2.7 Parameters for details on the structure.

When setting the slave address, store it without shifting 1 bit to left.

For the parameter which has '(to be updated)' in the comment below, the argument for the parameter will be updated during the API execution.

```
uint8_t * p_slv_adr; /* Pointer to the buffer to store the slave address */
uint8_t * p_data1st; /* Pointer to the buffer to store the first data */
uint8_t * p_data2nd; /* Pointer to the buffer to store the second data */
sci_iic_ch_dev_status_t dev_sts; /* Device state flag (to be updated) */
uint32_t cnt1st; /* First data counter (number of bytes)
                  (to be updated for only pattern 1) */
uint32_t cnt2nd; /* Second data counter (number of bytes)
                  (to be updated for only pattern 1 and 2) */
sci_iic_callback callbackfunc; /* Callback function */
uint8_t ch_no; /* Channel number */
```

Return Values

```
SCI_IIC_SUCCESS /* Processing completed successfully */
SCI_IIC_ERR_INVALID_CHAN /* The channel is nonexistent. */
SCI_IIC_ERR_INVALID_ARG /* The parameter is invalid. */
SCI_IIC_ERR_NO_INIT /* Uninitialized state */
SCI_IIC_ERR_BUS_BUSY /* The bus state is busy. */
SCI_IIC_ERR_OTHER /* The event occurred is invalid in the current state. */
```

Properties

Prototyped in r_sci_iic_rx_if.h.

Description

Starts the simple I²C-bus master transmission. The transmission is performed with the SCI channel and transmit pattern specified by parameters. If the state of the channel is 'idle (SCI_IIC_IDEL)', the following processes are performed.

- Setting the state flag
- Initializing variables used by the API
- Enabling the SCI interrupts
- Releasing the I²C reset
- Allocating I²C output ports
- Generating a start condition

Reentrant

Function is reentrant for different channels.

Example

- Case1: Transmit pattern 1

```
#include <stddef.h> // NULL definition
#include "platform.h"
#include "r_sci_iic_rx_if.h"

void main(void);
void Callback_ch1(void);

void main(void)
{
    volatile sci_iic_return_t ret;
    sci_iic_info_t siic_info;

    uint8_t slave_addr_eeprom[1] = {0x50}; /* Slave address for EEPROM */
    uint8_t access_addr1[1] = {0x00}; /* 1st data field */
    uint8_t send_data[5] = {0x81, 0x82, 0x83, 0x84, 0x85};

    /* Sets IIC Information (Send pattern 1) */
    siic_info.p_slv_adr = slave_addr_eeprom;
    siic_info.p_data1st = access_addr1;
    siic_info.p_data2nd = send_data;
    siic_info.dev_sts = 0;
    siic_info.cnt1st = 1;
    siic_info.cnt2nd = 3;
    siic_info.callbackfunc = &Callback_ch1;
    siic_info.ch_no = 1;

    /* SCI open */
    ret = R_SCI_IIC_Open(&siic_info);
    /* Start Master Send */
    ret = R_SCI_IIC_MasterSend(&siic_info);
    while(1);
}
```

```
void Callback_ch1(void)
{
    volatile sci_iic_return_t ret;
    sci_iic_mcu_status_t iic_status;
    sci_iic_info_t iic_info_ch;

    iic_info_ch.ch_no = 1;
    ret = R_SCI_IIC_GetStatus(&iic_info_ch, &iic_status);

    if (SCI_IIC_SUCCESS != ret)
    {
        /* Call error processing for the R_SCI_IIC_GetStatus() function*/
    }
    else
    {
        {
            if (1 == iic_status.BIT.NACK)
            {
                /* Processing when a NACK is detected
                 by verifying the iic_status flag. */
            }
        }
    }
}
```

- Case2: Transmitting data to two slave devices (Slave 1 and slave 2) continuously.

```
#include <stddef.h> // NULL definition
#include "platform.h"
#include "r_sci_iic_rx_if.h"
```

```
void main(void);
void Callback_ch1(void);
```

```
void main(void)
{
    volatile sci_iic_return_t ret;
    sci_iic_info_t siic_info;

    uint8_t slave_addr_eeprom[1] = {0x50}; /* Slave address for EEPROM */
    uint8_t slave_addr_m16c[1] = {0x01}; /* Slave address for M16C */
    uint8_t write_addr_slave1[1] = {0x01}; /* 1st data field */
    uint8_t write_addr_slave2[1] = {0x02}; /* 1st data field */
    uint8_t data_area_slave1[5] = {0x81,0x82,0x83,0x84,0x85};
    uint8_t data_area_slave2[5] = {0x18,0x28,0x38,0x48,0x58};
}
```

```

/* Sets 'Slave 1' Information (Send pattern 1) */
siic_info.p_slv_adr = slave_addr_eeprom;
siic_info.p_data1st = write_addr_slave1;
siic_info.p_data2nd = data_area_slave1;
siic_info.dev_sts = 0;
siic_info.cnt1st = 1;
siic_info.cnt2nd = 3;
siic_info.callbackfunc = &Callback_ch1;
siic_info.ch_no = 1;

```

```

/* SCI open */
ret = R_SCI_IIC_Open(&siic_info);
/* Start Master Send */
ret = R_SCI_IIC_MasterSend(&siic_info);

while((SCI_IIC_FINISH != siic_info.dev_sts) &&
      (SCI_IIC_NACK != siic_info.dev_sts));

```

```

/* Sets 'Slave 2' Information (Send pattern 1) */
siic_info.p_slv_adr = slave_addr_m16c;
siic_info.p_data1st = write_addr_slave2;
siic_info.p_data2nd = data_area_slave2;
siic_info.dev_sts = 0;
siic_info.cnt1st = 1;
siic_info.cnt2nd = 3;
siic_info.callbackfunc = &Callback_ch1;
siic_info.ch_no = 1;

```

```

/* Start Master Send */
ret = R_SCI_IIC_MasterSend(&siic_info);

while((SCI_IIC_FINISH != siic_info.dev_sts) &&
      (SCI_IIC_NACK != siic_info.dev_sts));
while(1);
}
void Callback_ch1(void)
{
    volatile sci_iic_return_t ret;
    sci_iic_mcu_status_t iic_status;
    sci_iic_info_t iic_info_ch;

    iic_info_ch.ch_no = 1;
    ret = R_SCI_IIC_GetStatus(&iic_info_ch, &iic_status);

    if (SCI_IIC_SUCCESS != ret)
    {
        /* Call error processing for the R_SCI_IIC_GetStatus() function*/
    }
    else
    {
        if (1 == iic_status.BIT.NACK)
        {
            /* Processing when a NACK is detected
             by verifying the iic_status flag. */
        }
    }
}

```

To access multiple slave devices,
rewrite the information structure for
each slave device to be accessed.

Special Notes

The table below lists available settings for each pattern.

Structure Member	Available Settings for Each Pattern of the Master Transmission			
	Pattern 1	Pattern 2	Pattern 3	Pattern 4
*p_slv_adr	Buffer pointer to the slave address storage			FIT_NO_PTR ⁽¹⁾
*p_data1st	Buffer pointer to the first data storage	FIT_NO_PTR ⁽¹⁾	FIT_NO_PTR ⁽¹⁾	FIT_NO_PTR ⁽¹⁾
*p_data2nd	Buffer pointer to the second data (transmit data) storage		FIT_NO_PTR ⁽¹⁾	FIT_NO_PTR ⁽¹⁾
dev_sts	Device state flag			
cnt1st	0000 0001h to FFFF FFFFh ⁽²⁾	0	0	0
cnt2nd	0000 0001h to FFFF FFFFh ⁽²⁾		0	0
callbackfunc	Specify the function name used			
ch_no	00h to FFh			
rsv1, rsv2, rsv3	Reserved (value set here has no effect)			

Notes:

1. When using pattern 2, 3, or 4, set 'FIT_NO_PTR' as the argument of the parameter.
2. Do not set to 0.

3.3 R_SCI_IIC_MasterReceive()

This function is used when the master reception starts.

Format

```
sci_iic_return_t R_SCI_IIC_MasterReceive(
    sci_iic_info_t * p_sci_iic_info /* Structure data */
)
```

Parameters

**p_sci_iic_info*

This is the pointer to the I²C communication information structure. The receive pattern can be selected from master reception and master composite. Refer to the Special Notes in this section for available settings and the setting values for each receive pattern. Also refer to 1.3.3 Master Reception for details of each receive pattern.

Only members of the structure used in this function are described here. Refer to 2.7 Parameters for details on the structure.

When setting the slave address, store it without shifting 1 bit to left.

For the parameter which has ‘(to be updated)’ in the comment below, the argument for the parameter will be updated during the API execution.

```
uint8_t * p_slv_adr; /* Pointer to the buffer to store the slave address */
uint8_t * p_data1st; /* Pointer to the buffer to store the first data */
uint8_t * p_data2nd; /* Pointer to the buffer to store the second data */
sci_iic_ch_dev_status_t dev_sts; /* Device state flag (to be updated) */
uint32_t cnt1st; /* First data counter (number of bytes) */
                (to be updated only for master composite) */
uint32_t cnt2nd; /* Second data counter (number of bytes) (to be updated) */
sci_iic_callback callbackfunc; /* Callback function */
uint8_t ch_no; /* Channel number */
```

Return Values

```
SCI_IIC_SUCCESS /* Processing completed successfully */
SCI_IIC_ERR_INVALID_CHAN /* The channel is nonexistent. */
SCI_IIC_ERR_INVALID_ARG /* The parameter is invalid. */
SCI_IIC_ERR_NO_INIT /* Uninitialized state */
SCI_IIC_ERR_BUS_BUSY /* The bus state is busy. */
SCI_IIC_ERR_OTHER /* The event occurred is invalid in the current state. */
```

Properties

Prototyped in r_sci_iic_rx_if.h.

Description

Starts the simple I²C-bus master reception. The reception is performed with the SCI channel and receive pattern specified by parameters. If the state of the channel is ‘idle (SCI_IIC_IDEL)’, the following processes are performed.

- Setting the state flag
- Initializing variables used by the API
- Enabling the SCI interrupts
- Releasing the I²C reset
- Allocating I²C output ports
- Generating a start condition

Reentrant

Function is reentrant for different channels.

Example

```
/* Sample: MasterReceive (Combination mode) */
#include <stddef.h> // NULL definition
#include "platform.h"
#include "r_sci_iic_rx_if.h"

void main(void);
void Callback_ch1(void);

void main(void)
{
    volatile sci_iic_return_t ret;
    sci_iic_info_t siic_info;

    uint8_t slave_addr_eeprom[1] = {0x50}; /* Slave address for EEPROM */
    uint8_t access_addr1[1] = {0x00}; /* 1st data field */
    uint8_t store_area[5] = {0xFF,0xFF,0xFF,0xFF,0xFF};

    /* Sets IIC Information (Ch1) */
    siic_info.p_slv_adr = slave_addr_eeprom;
    siic_info.p_data1st = access_addr1;
    siic_info.p_data2nd = store_area;
    siic_info.dev_sts = 0;
    siic_info.cnt1st = 1;
    siic_info.cnt2nd = 3;
    siic_info.callbackfunc = &Callback_ch1;
    siic_info.ch_no = 1;

    /* SCI open */
    ret = R_SCI_IIC_Open(&siic_info);
    /* Start Master Receive */
    ret = R_SCI_IIC_MasterReceive(&siic_info);
    while(1);
}

void Callback_ch1(void)
{
    volatile sci_iic_return_t ret;
    sci_iic_mcu_status_t iic_status;
    sci_iic_info_t iic_info_ch;

    iic_info_ch.ch_no = 1;
    ret = R_SCI_IIC_GetStatus(&iic_info_ch, &iic_status);

    if (SCI_IIC_SUCCESS != ret)
    {
        /* Call error processing for the R_SCI_IIC_GetStatus() function*/
    }
}
```

```

else
{
    if (1 == iic_status.BIT.NACK)
    {
        /* Processing when a NACK is detected
        by verifying the iic_status flag. */
    }
}
}

```

Special Notes

The table below lists available settings for each receive pattern.

Structure Member	Available Settings for Each Pattern of the Master Reception	
	Master Reception	Master Composite
*p_slv_adr	Buffer pointer to the slave address storage	
*p_data1st	(Value set here has no effect)	Buffer pointer to the first data storage
*p_data2nd	Buffer pointer to the second data (receive data) storage	
dev_sts	Device state flag	
cnt1st ⁽¹⁾	0	0000 0001h to FFFF FFFFh
cnt2nd ⁽²⁾	0000 0001h to FFFF FFFFh	0000 0001h to FFFF FFFFh
callbackfunc	Specify the function name used	
ch_no	00h to FFh	
rsv1, rsv2, rsv3	Reserved (value set here has no effect)	

Notes:

1. The receive pattern is determined by whether cnt1st is 0 or not.
2. Do not set to 0.

3.4 R_SCI_IIC_Close()

This function is used when completing the simple I²C communication and releasing the SCI used.

Format

```
sci_iic_return_t R_SCI_IIC_Close(  
    sci_iic_info_t * p_sci_iic_info /* Structure data */  
)
```

Parameters

**p_sci_iic_info*

This is the pointer to the I²C communication information structure.

Only the member of the structure used in this function is described here. Refer to 2.7 Parameters for details on the structure.

For the parameter which has '(to be updated)' in the comment below, the argument for the parameter will be updated during the API execution.

```
sci_iic_ch_dev_status_t dev_sts; /* Device state flag (to be updated) */  
uint8_t ch_no; /* Channel number */
```

Return Values

```
SCI_IIC_SUCCESS /* Processing completed successfully */  
SCI_IIC_ERR_INVALID_CHAN /* The channel is nonexistent. */  
SCI_IIC_ERR_INVALID_ARG /* The parameter is invalid. */
```

Properties

Prototyped in r_sci_iic_rx_if.h.

Description

Configures the settings to complete the simple I²C-bus communication. Disables the SCI channel specified by the parameter. The following processes are performed in this function.

- Entering the SCI module-stop state
- Releasing I²C output ports
- Disabling the SCI interrupt

To restart the communication, call the R_SCI_IIC_Open() function (initialization function). If the communication is forcibly terminated, that communication is not guaranteed.

Reentrant

Function is reentrant for different channels.

Example

```
volatile sci_iic_return_t  ret;  
sci_iic_info_t            siic_info;  
  
siic_info.ch_no = 1;  
  
ret = R_SCI_IIC_Close(&siic_info);
```

Special Notes

None

3.5 R_SCI_IIC_GetStatus()

This function is used when verifying the state of this module.

Format

```
sci_iic_return_t R_SCI_IIC_GetStatus(
    sci_iic_info_t * p_sci_iic_info /* Structure data */
    sci_iic_sts_flg_t *p_sci_iic_status /* State of this module */
)
```

Parameters

*p_sci_iic_info

This is the pointer to the I²C communication information structure.

Only the member of the structure used in this function is described here. Refer to 2.7 Parameters for details on the structure.

```
uint8_t ch_no; /* Channel number */
```

*p_sci_iic_status

This contains the address to store the I²C state flag. If the argument is 'FIT_NO_PTR', the state is not returned.

Use the structure members listed below to specify parameters.

```
typedef union
{
    uint32_t LONG;
    struct st_sci_iic_status_flag
    {
        uint32_t rsv :27 /* Reserve bit */
        uint32_t SCLI:1; /* SSCL pin level */
        uint32_t SDAI:1; /* SSDA pin level */
        uint32_t NACK :1; /* NACK detection flag */
        uint32_t TRS :1; /* Transmit/receive mode level */
        uint32_t BSY :1; /* Bus state flag */
    }BIT;
} sci_iic_mcu_status_t;
```

Return Values

SCI_IIC_SUCCESS / Processing completed successfully */*

SCI_IIC_ERR_INVALID_CHAN / The channel is nonexistent. */*

SCI_IIC_ERR_INVALID_ARG / The parameter is invalid. */*

SCI_IIC_ERR_OTHER / The event occurred is invalid in the current state. */*

Properties

Prototyped in r_sci_iic_rx_if.h.

Description

Returns the state of this module.

By reading the register, pin level, variable, or others, obtains the state of the SCI channel which specified by the parameter, and returns the obtained state as 32-bit structure.

Reentrant

Function is reentrant for different channels.

Example

```
volatile sci_iic_return_t      ret;
sci_iic_info_t                siic_info;
sci_iic_mcu_status_t          iic_status;

siic_info.ch_no = 1

ret = R_SCI_IIC_GetStatus(&siic_info, &status_add);
```

Special Notes

The following shows the state flag allocation.

b31 to b16
Reserved
Reserved
rsv
Always 0

b15 to b8
Reserved
Reserved
rsv
Always 0

b7 to b5	b4	b3	b2	b1	b0
Reserved	Pin level		Event detection	Mode	Bus state
Reserved	SSCL pin level	SSDA pin level	NACK detection	Send/receive mode	Bus busy/ready
rsv	SCLI	SDAI	NACK	TRS	BSY
Always 0	0: Low level 1: High level		0: Not detected 1: Detected	0: Receive 1: Transmit	0: Idle 1: Busy

3.6 R_SCI_IIC_Control()

This function is mainly used when a communication error occurs.

It outputs conditions, Hi-Z from the SSDA pin, and one-shot of the SSCL clock. Also it resets the settings of this module.

Format

```
sci_iic_return_t R_SCI_IIC_Control(
    r_sci_iic_info_t * p_sci_iic_info /* Structure data */
    sci_iic_ctrl_ptn_t ctrl_ptn /* Output pattern */
);
```

Parameters

*p_sci_iic_info

This is the pointer to the I²C communication information structure.

Only the member of the structure used in this function is described here. Refer to 2.7 Parameters for details on the structure.

For the parameter which has ‘(to be updated)’ in the comment below, the argument for the parameter will be updated during the API execution.

```
sci_iic_ch_dev_status_t dev_sts; /* Device state flag (to be updated) */
uint8_t ch_no; /* Channel number */
```

ctrl_ptn_t

Specifies the output pattern. When selecting multiple options, specify them with ‘|’.

The following options can be selected simultaneously:

- The following three options can be specified simultaneously. Then they will be processed in the order listed.

- SCI_IIC_GEN_START_CON
- SCI_IIC_GEN_RESTART_CON
- SCI_IIC_GEN_STOP_CON

- The following two options can be specified simultaneously.

- SCI_IIC_GEN_SDA_HI_Z
- SCI_IIC_GEN_SSCL_ONESHOT

```
typedef uint8_t sci_iic_ctrl_ptn_t;
#define SCI_IIC_GEN_START_CON (sci_iic_ctrl_ptn_t) (0x01)
/* Start condition generation */
#define SCI_IIC_GEN_STOP_CON (sci_iic_ctrl_ptn_t) (0x02)
/* Stop condition generation */
#define SCI_IIC_GEN_RESTART_CON (sci_iic_ctrl_ptn_t) (0x04)
/* Restart condition generation */
#define SCI_IIC_GEN_SSDA_HI_Z (sci_iic_ctrl_ptn_t) (0x08)
/* Hi-Z output from the SSDA pin */
#define SCI_IIC_GEN_SSCL_ONESHOT (sci_iic_ctrl_ptn_t) (0x10)
/* SSCL clock one-shot output */
#define SCI_IIC_GEN_RESET (sci_iic_ctrl_ptn_t) (0x20)
/* Simple I2C mode reset */
```

Return Values

SCI_IIC_SUCCESS /* Processing completed successfully */
SCI_IIC_ERR_INVALID_CHAN /* The channel is nonexistent. */
SCI_IIC_ERR_INVALID_ARG /* The parameter is invalid. */
SCI_IIC_ERR_BUS_BUSY /* The bus state is busy. */
SCI_IIC_ERR_OTHER /* The event occurred is invalid in the current state. */

Properties

Prototyped in r_sci_iic_rx_if.h.

Description

Outputs control signals of the simple I²C mode. Outputs conditions specified by the argument, Hi-Z from the SSDA pin, and one-shot of the SSCL clock. Also resets the simple I²C mode settings.

Reentrant

Function is reentrant for different channels.

Example

```
volatile sci_iic_return_t    ret;  
sci_iic_info_t              siic_info;  
  
siic_info.ch_no = 1;  
  
/* Output an extra SSCL clock cycle after changes the SSDA pin in a high-  
impedance state */  
ret = R_SCI_IIC_Control(&siic_info, SCI_IIC_GEN_SSDA_HI_Z |  
SCI_IIC_SSCL_ONESHOT);
```

Special Notes

None

3.7 R_SCI_IIC_GetVersion()

This function returns the API version.

Format

uint32_t R_SCI_IIC_GetVersion(void)

Parameters

None

Return Values

Version number

Properties

Prototyped in r_sci_iic_rx_if.h.

Description

Returns the API version number.

Reentrant

Function is reentrant for different channels.

Example

```
uint32_t version;  
  
version = R_SCI_IIC_GetVersion();
```

Special Notes

This function is inlined using '#pragma inline'.

4. Appendices

4.1 Communication Method

This API controls each processing such as start condition generation, slave address transmission, and others as a single protocol, and performs communication by combining these protocols.

4.1.1 States for API Operation

Table 4.1 lists the States Used for Protocol Control.

Table 4.1 States Used for Protocol Control (enum sci_iic_api_status_t)

No.	Constant Name	Description
STS0	SCI_IIC_STS_NO_INIT	Uninitialized state
STS1	SCI_IIC_STS_IDLE	Idle state
STS2	SCI_IIC_STS_ST_COND_WAIT	Wait state for a start condition to be generated
STS3	SCI_IIC_STS_SEND_SLVADR_W_WAIT	Wait state for the slave address [write] transmission to complete
STS4	SCI_IIC_STS_SEND_SLVADR_R_WAIT	Wait state for the slave address [read] transmission to complete
STS5	SCI_IIC_STS_SEND_DATA_WAIT	Wait state for the data transmission to complete
STS6	SCI_IIC_STS_RECEIVE_DATA_WAIT	Wait state for the data reception to complete
STS7	SCI_IIC_STS_SP_COND_WAIT	Wait state for a stop condition to be generated

4.1.2 Events During API Operation

Table 4.2 lists the Events Used for Protocol Control. When the interface functions accompanying this module are called, they are defined as events as well as interrupts.

Table 4.2 Events Used for Protocol Control (enum sci_iic_api_event_t)

No.	Event	Event Definition
EV0	SCI_IIC_EV_INIT	sci_iic_init_driver() called
EV1	SCI_IIC_EV_GEN_START_COND	sci_iic_generate_start_cond() called
EV2	SCI_IIC_EV_INT_START	STI interrupt occurred (interrupt flag: START)
EV3	SCI_IIC_EV_INT_ADD	TXI interrupt occurred
EV4	SCI_IIC_EV_INT_SEND	TXI interrupt occurred
EV5	SCI_IIC_EV_INT_STOP	STI interrupt occurred (interrupt flag: STOP)
EV6	SCI_IIC_EV_INT_NACK	STI interrupt occurred (interrupt flag: NACK)

4.1.3 Protocol State Transitions

In this module, a state transition occurs when an interface function provided is called or when an I²C interrupt request is generated. Figure 4.1 to Figure 4.4 show protocol state transitions.

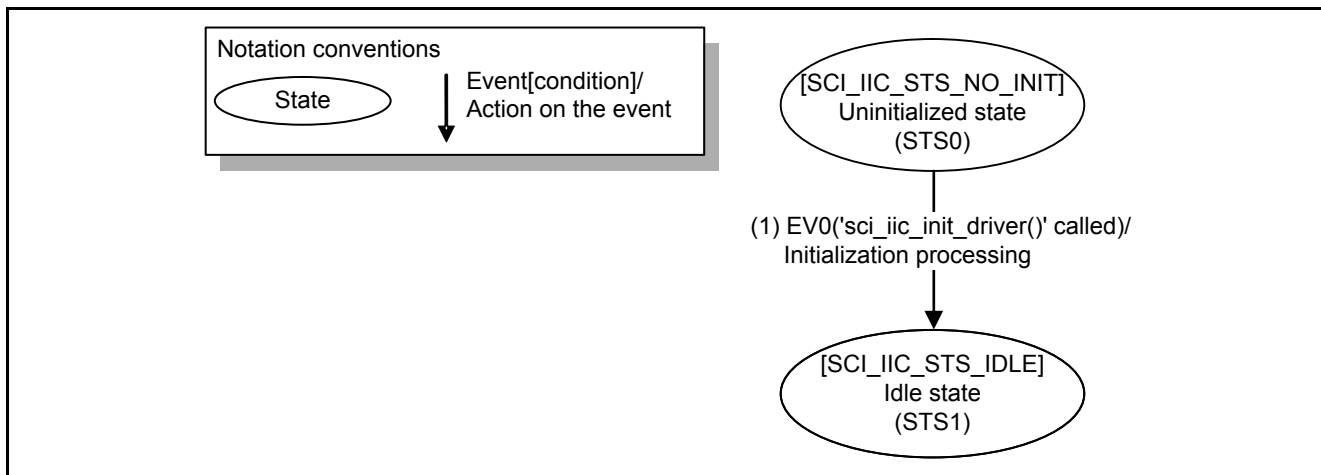


Figure 4.1 State Transition on Initialization

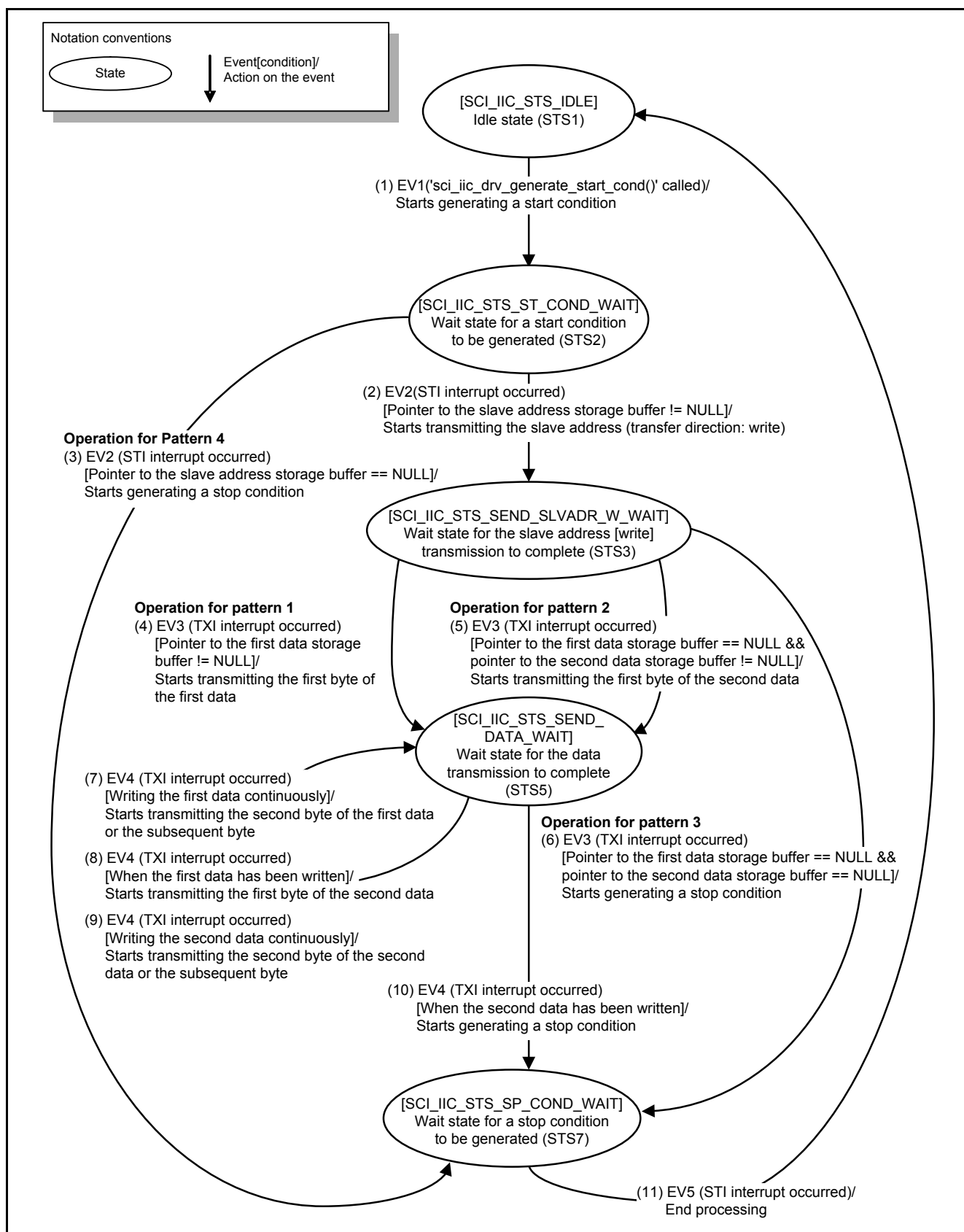


Figure 4.2 State Transition on Master Transmission

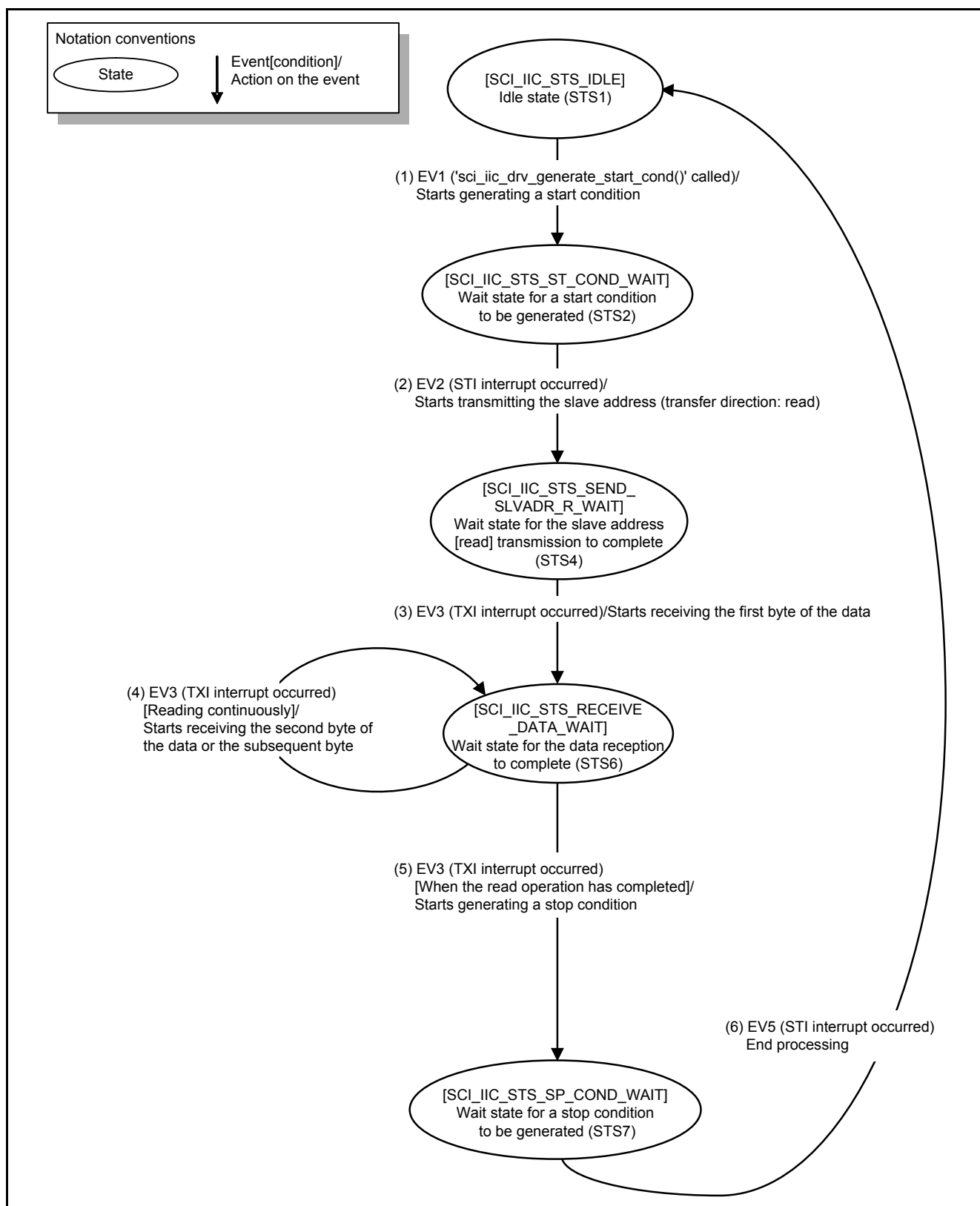


Figure 4.3 State Transition on Master Reception

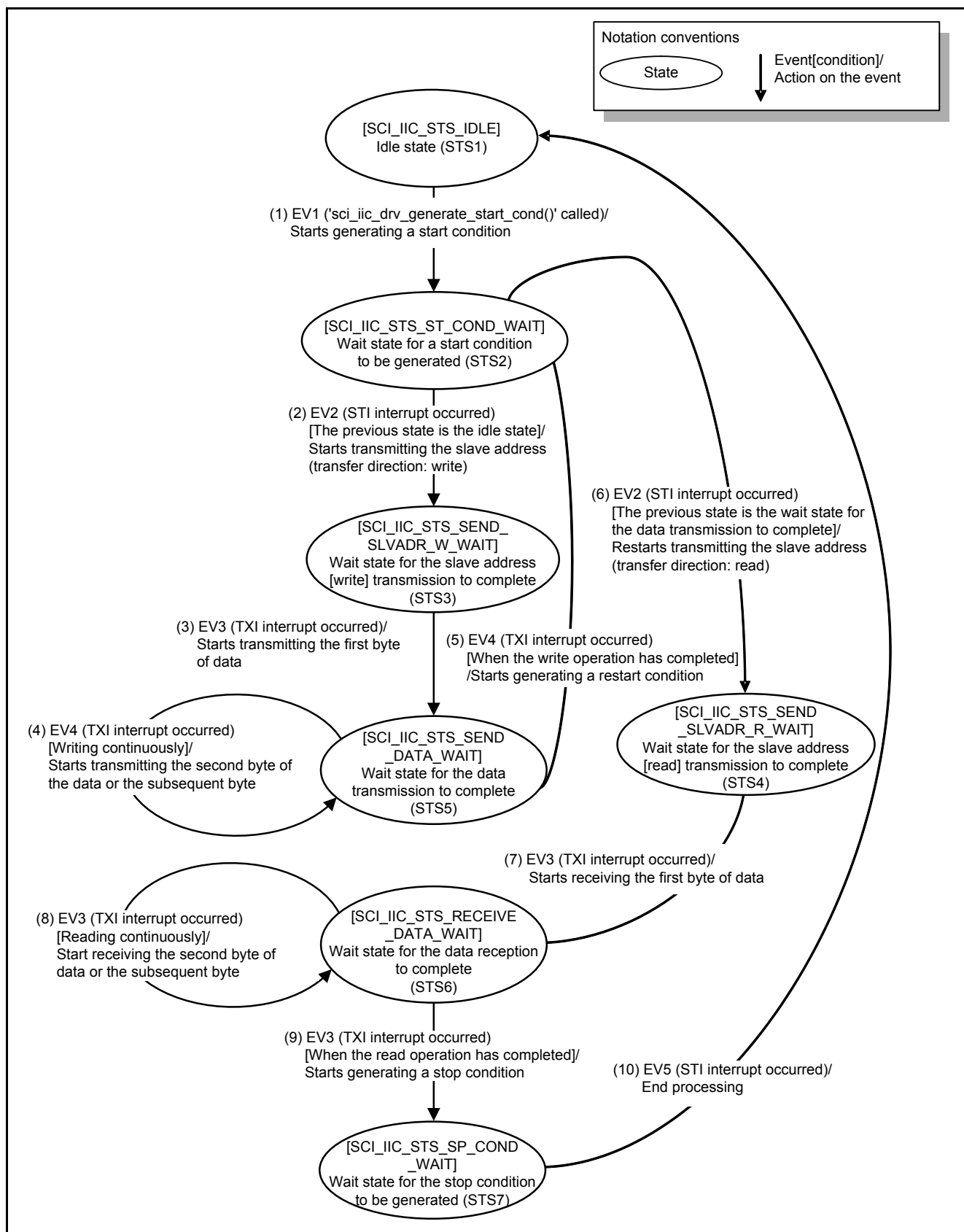


Figure 4.4 State Transition on Master Composite

4.1.4 Protocol State Transition Table

The processing when the events in Table 4.2 occur in the states in Table 4.1 is shown in the Table 4.3 Protocol State Transition. Refer to Table 4.4 for details of each function.

Table 4.3 Protocol State Transition Table (gc_sci_iic_mtx_tbl[]) ⁽¹⁾

State		Event						
		EV0	EV1	EV2	EV3	EV4	EV5	EV6
STS0	Uninitialized state [SCI_IIC_STS_NO_INIT]	Func0	ERR	ERR	ERR	ERR	ERR	ERR
STS1	Idle state [SCI_IIC_STS_IDLE]	ERR	Func1	ERR	ERR	ERR	ERR	ERR
STS2	Wait state for a start condition to be generated [SCI_IIC_STS_ST_COND_WAIT]	ERR	ERR	Func2	ERR	ERR	ERR	Func7
STS3	Wait state for the slave address [write] transmission to complete [SCI_IIC_STS_SEND_SLVADR_W_WAIT]	ERR	ERR	ERR	Func3	ERR	ERR	Func7
STS4	Wait state for the slave address [read] transmission to complete [SCI_IIC_STS_SEND_SLVADR_R_WAIT]	ERR	ERR	ERR	Func3	ERR	ERR	Func7
STS5	Wait state for the data transmission to complete [SCI_IIC_STS_SEND_DATA_WAIT]	ERR	ERR	ERR	ERR	Func4	ERR	Func7
STS6	Wait state for the data reception to complete [SCI_IIC_STS_RECEIVE_DATA_WAIT]	ERR	ERR	ERR	Func5	ERR	ERR	Func7
STS7	Wait state for the stop condition to be generated [SCI_IIC_STS_SP_COND_WAIT]	ERR	ERR	ERR	ERR	ERR	Func6	Func7

Note:

1. ERR indicates SCI_IIC_ERR_OTHER. When an unexpected event is notified in a state, error processing will be performed.

4.1.5 Functions Used on Protocol State Transitions

Table 4.4 lists the Functions Used on Protocol State Transition.

Table 4.4 Functions Used on Protocol State Transition

Processing	Function	Overview
Func0	sci_iic_init_driver()	Initialization
Func1	sci_iic_generate_start_cond()	Start condition generation
Func2	sci_iic_after_gen_start_cond()	Processing after generating a start condition
Func3	sci_iic_after_send_slvadr()	Processing after transmitting the slave address
Func4	sci_iic_write_data_sending()	Data transmission
Func5	sci_iic_read_data_receiving()	Data reception
Func6	sci_iic_release()	Communication end processing
Func7	sci_iic_nack()	NACK error processing

4.1.6 Flag States on State Transitions

1) Controlling states of channels

Multiple slaves on the same bus can be exclusively controlled using the channel state flag 'g_sci_iic_ChStatus[]'. Each channel has the channel state flag and the flag is controlled by the global variable. When the initialization for this module has completed and the target bus is not being used for a communication, the flag becomes 'SCI_IIC_IDLE/SCI_IIC_FINISH/SCI_IIC_NACK' (idle state) and communication is available. When the bus is being used for communication, the flag becomes 'SCI_IIC_COMMUNICATION' (communicating). When communication is started, the flag is always verified. Thus, if a device is communicating on a bus, then no other device can start communicating on the same bus. Simultaneous communication can be achieved by controlling the channel state flag for each channel.

2) Controlling states of devices

Multiple slaves on the same channel can be controlled using the device state flag 'dev_sts' in the I²C communication information structure. The device state flag stores the state of communication for the device.

Table 4.5 lists States of Flags on State Transitions.

Table 4.5 States of Flags on State Transitions

State	Channel State Flag	Device State Flag (Communication Device)	I ² C Protocol Operating Mode	Current State of the Protocol Control
	g_sci_iic_ChStatus[]	I ² C Communication Information Structure *p_dev_sts	Internal Communication Information Structure api_Mode	Internal Communication Information Structure api_N_status
Uninitialized state	SCI_IIC_NO_INIT	SCI_IIC_NO_INIT	SCI_IIC_MODE_NONE	SCI_IIC_STS_NO_INIT
Idle state	SCI_IIC_IDLE	SCI_IIC_IDLE	SCI_IIC_MODE_NONE	SCI_IIC_STS_IDLE
	SCI_IIC_FINISH	SCI_IIC_FINISH		
	SCI_IIC_NACK	SCI_IIC_NACK		
Communicating (master transmission)	SCI_IIC_ COMMUNICATION	SCI_IIC_ COMMUNICATION	SCI_IIC_MODE_WRITE	SCI_IIC_STS_ST_COND_WAIT
				SCI_IIC_STS_SEND_SLVADR_W_WAIT
				SCI_IIC_STS_SEND_DATA_WAIT
				SCI_IIC_STS_SP_COND_WAIT
Communicating (master reception)	SCI_IIC_ COMMUNICATION	SCI_IIC_ COMMUNICATION	SCI_IIC_MODE_READ	SCI_IIC_STS_ST_COND_WAIT
				SCI_IIC_STS_SEND_SLVADR_R_WAIT
				SCI_IIC_STS_RECEIVE_DATA_WAIT
				SCI_IIC_STS_SP_COND_WAIT
Communicating (master composite)	SCI_IIC_ COMMUNICATION	SCI_IIC_ COMMUNICATION	SCI_IIC_MODE_ COMBINED	SCI_IIC_STS_ST_COND_WAIT
				SCI_IIC_STS_SEND_SLVADR_W_WAIT
				SCI_IIC_STS_SEND_SLVADR_R_WAIT
				SCI_IIC_STS_SEND_DATA_WAIT
				SCI_IIC_STS_RECEIVE_DATA_WAIT
				SCI_IIC_STS_SP_COND_WAIT
Error state	SCI_IIC_ERROR	SCI_IIC_ERROR	—	—

4.2 Interrupt Request Generation Timing

This section describes the interrupt request generation timings in this module.

Legend:

ST: Start condition

AD6 to AD0: Slave address

/W: Transfer direction bit: 0 (Write)

R: Transfer direction bit: 1 (Read)

/ACK: Acknowledge: 0

NACK: Acknowledge: 1

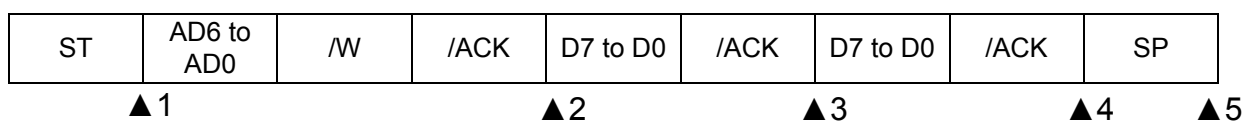
D7 to D0: Data

RST: Restart condition

SP: Stop condition

4.2.1 Master Transmission

(1) Pattern 1



▲ 1: STI (START) interrupt: Start condition detected

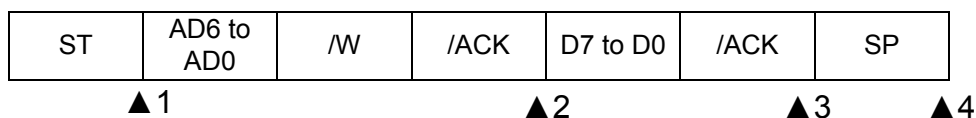
▲ 2: TXI interrupt: Address transmission completed (transfer direction bit: write) ⁽¹⁾

▲ 3: TXI interrupt: Data transmission completed (first data) ⁽¹⁾

▲ 4: TXI interrupt: Data transmission completed (second data) ⁽¹⁾

▲ 5: STI (STOP) interrupt: Stop condition detected

(2) Pattern 2



▲ 1: STI (START) interrupt: Start condition detected

▲ 2: TXI interrupt: Address transmission completed (transfer direction bit: write) ⁽¹⁾

▲ 3: TXI interrupt: Data transmission completed (second data) ⁽¹⁾

▲ 4: STI (STOP) interrupt: Stop condition detected

Note:

1. An interrupt request is generated on the rising edge of the ninth clock.

ST	AD6 to AD0	/W	/ACK	SP
▲ 1			▲ 2	▲ 3

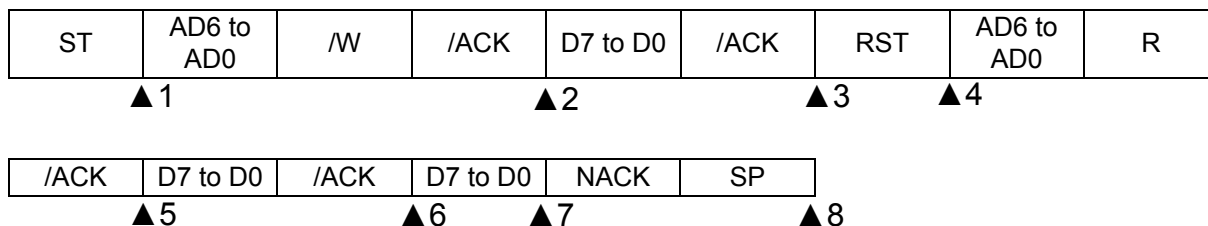
- | | |
|----|----|
| ST | SP |
|----|----|
- ▲1

▲2

- | | | | | | | | | |
|-----|------------|-----|------|----------|------|----------|------|-----|
| ST | AD6 to AD0 | R | /ACK | D7 to D0 | /ACK | D7 to D0 | NACK | SP |
| ▲ 1 | | ▲ 2 | | ▲ 3 | | ▲ 4 | | ▲ 5 |

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4.2.3 Master Composite



▲ 1: STI (START) interrupt: Start condition detected

▲ 2: TXI interrupt: Address transmission completed (transfer direction bit: write) ⁽¹⁾

▲ 3: TXI interrupt: Data transmission completed (first data) ⁽¹⁾

▲ 4: STI (START) interrupt: Restart condition detected

▲ 5: TXI interrupt: Address transmission completed (transfer direction bit: read) ⁽¹⁾

▲ 6: TXI interrupt: Reception for the last data - 1 completed (second data) ⁽¹⁾

▲ 7: TXI interrupt: Reception for the last data completed (second data) ⁽²⁾

▲ 8: STI (STOP) interrupt: Stop condition detected

Notes:

1. An interrupt request is generated on the rising edge of the ninth clock.
2. An interrupt request is generated on the rising edge of the eighth clock.

5. Provided Modules

The module provided can be downloaded from the Renesas Electronics website.

6. Reference Documents

User's Manual: Hardware

The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

User's Manual: Development Tools

RX Family C/C++ Compiler Package V.1.01 User's Manual Rev.1.00 (R20UT0570EJ)

The latest version can be downloaded from the Renesas Electronics website.

Website and Support

Renesas Electronics website

<http://www.renesas.com>

Inquiries

<http://www.renesas.com/contact/>

REVISION HISTORY	RX Family Application Note Simple I ² C Module Using Firmware Integration Technology
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Rev.	Date	Description	
		Page	Summary
1.00	July 1, 2013	—	First edition issued
1.10	Nov. 15, 2013	—	Modified return values.
1.20	July 1, 2014	1	Target Device: Added the RX100 Series support.
		4	Table 1.2 Required Memory Size: - Changed all memory sizes in association with additional support for the RX100 Series and additional function for port selection. - Modified the description of the first sentence below the table.
		13	2.3 Supported Toolchains: Updated the toolchain version to v.2.01.
		15	2.6 Configuration Overview (Configuration options in r_sci_iic_rx_config.h (2/2)): Added the configuration option definitions in association with additional function for port selection.
		17	2.9 Adding the FIT Module to Your Project: Modified the description.
1.30	Aug. 25, 2014	—	Added support for the RX113 Group and RX64M Group.
		1	Target Device: Changed according to the products supported.
		1	Added the “Related Documents”.
		3	Limitations: Added three limitation items.
		4	Table 1.2 Required Memory Size: Modified the memory sizes for the ROM, Maximum user stack usage, and Maximum interrupt stack usage.
		13	2.2 Software Requirements: Deleted “r_cgc_rx” since this module is independent of the r_cgc_rx.
		14-16	Configuration Overview: - Added channel support for the configuration options. Channels supported: 0 to 9, 12 - Added the following configuration option: “SCI_IIC_CFG_PORT_SETTING_PROCESSING”.
		21, 26, 32	3.2 R_SCI_IIC_MasterSend(), 3.3 R_SCI_IIC_MasterReceive(), and 3.4 R_SCI_IIC_Close(): Modified the code in the Example sections.

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

- The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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Renesas Electronics Corporation

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Renesas Electronics America Inc.

2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited

1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH

Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.

Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.

Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited

Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852-2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.

13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886-2-8175-9670

Renesas Electronics Singapore Pte. Ltd.

80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jin Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.

12F., 234 Teheran-ro, Gangnam-Ku, Seoul, 135-920, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141