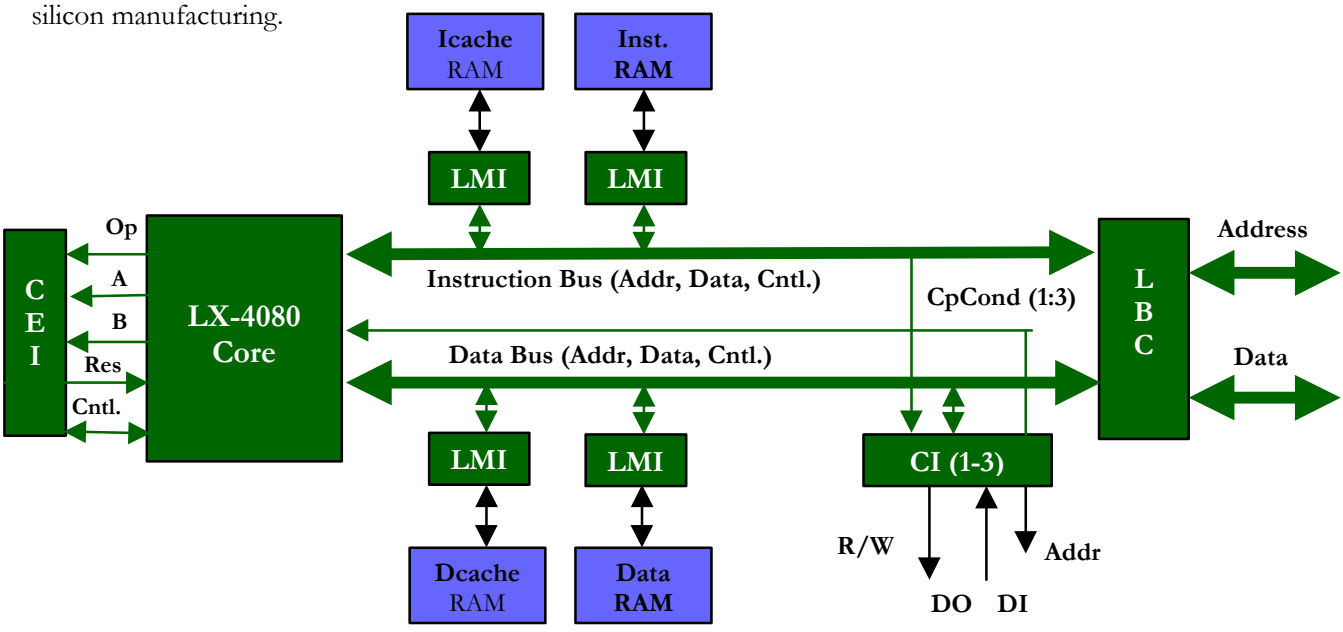
LEXRA	**High Performance** **32-Bit Embedded Processor**	**LX-4080** **Product Brief**

- **Best Price/Performance:** 100 MHz worst case and less than 2 mm^2 in 0.35 µ processes.
- **Executes MIPS-Iâ Instructions*:** Minimizes the porting effort for all third party software development tools.
- **Easy ASIC Design:** Single phase clocking, fully synchronous design, with easy to interface system bus protocol. Supports popular EDA tools.
- **Portability:** Easily portable RTL core and SmoothCore™ for popular COT foundries and ASIC vendors.
- **Easy Customization:** User-defined instructions, cache and RAM sizes, buffer sizes, as well as addressing space setting.

OVERVIEW

LX-4080 is an embedded RISC processor core targeted at system-on-silicon designers who require the best in price/performance and ease-of-use. Key applications include network products such as network protocol processors, cable modems, set-top boxes, as well as consumer products such as digital still cameras and inkjet printers..

In these high-volume products, cost and time-to-market are the two most critical issues for a design team. The LX-4080 addresses both concerns. The 2 mm^2 die size is substantially smaller than most MIPS R3000 based solutions, while the 133 MIPS delivers enough performance so that designers do not have to resort to expensive MIPS R4000 cores. The time-to-market advantage for the LX-4080 comes from Lexra s simple system level interface, complete software development tools, easy hardware design methodology, and flexible silicon manufacturing.



ARCHITECTURE OVERVIEW

The LX-4080 RISC processor executes the MIPS-I® instruction set*. However, the VLSI architecture is quite different from those of MIPS R3000 based RISC processors and processor cores. The clocking, pipeline structure, pin-out, memory architecture, and system level interfaces have all been designed to reflect system-on-silicon design needs, deep submicron process technology, as well as design methodology advances.

MIPS-ISA-Iâ *. The LX-4080 supports the MIPS I programming model. That is, the instruction set incorporates a three-port register file. Two source operands can be supplied and one destination updated per cycle. The second operand is either a register or 16-bit immediate. The instruction set includes a wide selection of ALU operations executed by the RALU, Lexra s proprietary register based ALU. The RALU also generates memory addresses for 8-bit, 16-bit and 32-bit register loads from (stores to) memory by adding a register base to an immediate offset. Branches are based on comparisons between registers, rather than flags, and are therefore easy to relocate. Optional links following jump or branch instructions assist with subroutine programming.

The MIPS unaligned load and store instructions are supported through software emulation, because these instructions are seldom used, hardwired implementation represents poor price/performance tradeoffs, and their absence does not affect the software programming model.

Pipeline. Instructions are executed by a five-stage pipeline, which has been engineered so that all transactions internal to the LX-4080 as well as at the interfaces, occur on the positive edge of the processor clock. Unlike most implementations, two-phase clocks are not used. As a result, designs based on the LX-4080 will achieve higher clock speeds in deep submicron technologies without having to use expensive phase lock loop (PLL) logic.

Exception Handling. The MIPS I exception handling model is supported. Exceptions include both instruction-synchronous *traps* as well as hardware and software *interrupts*. Exceptions are prioritized. When an exception is taken, a user program located at the exception vector identifies the cause of the exception, and transfers control to the application-specific handler.

Coprocessor Operations. The LX-4080 supports all 32-bit Coprocessor operations. These include moves to and from the Coprocessor general registers and control registers (MTCz, MFCz, CTCz, CFCz), Coprocessor loads and stores (LWCz, SWCz) and branches based on Coprocessor condition flags (BCzT, BCzF). The Lexra-supplied Coprocessor Interface can support all Coprocessor Operations in a single cycle, without pipeline stalls.

IMPLEMENTATION OVERVIEW

The implementation philosophy for the LX-4080 supports the objectives of achieving excellent price/performance and time-to-market. As such, Lexra provides two different methods of delivering the LX-4080: RTL Core and SmoothCore. They are aimed respectively at two different development and business models: ASIC & COT.

RTL Core: For ASIC designers, the RTL core is a fully scan-testable Verilog source code of the LX-4080, and can be targeted to any ASIC vendor s standard cell or gate array libraries. In this case, the designer can simply follow the ASIC vendor s design flow to ensure proper sign-off. In addition to the Verilog source code and system level testbench, Lexra provides synthesis scripts as well as floor plan guidelines to maximize the performance of the LX-4080.

Depending upon the particular 0.35µ process, the cell library, and the design methodology used, the RTL core should achieve at least 66 MHz operation.

SmoothCore: For COT designers who manufacture at popular foundries such as IBM, and UMC, SmoothCore is the quickest, lowest cost, and best performance choice. In this case, the LX-4080 has been fully implemented and verified as a hard macro. All datapath, register file, and interface optimizations have been performed to ensure the smallest die and fastest performance possible. Furthermore, there is a scan based test pattern which provides 99.5% fault coverage during manufacturing tests.

SmoothCore Delivery: Since SmoothCore is delivered as an implemented hard macro, most of the design database will be provided by Lexra. This includes:

- Encrypted Verilog RTL and gate level models
- Post-layout timing for the target process.
- Behavior model for Motive static timing analysis.
- Layout GDSII
- DRC/LVS result log file

SYSTEM LEVEL BUILDING BLOCKS

The LX-4080 is designed to easily fit into different target applications. In addition to the processor core, it also provides the following integration building blocks:

- A simple memory management unit (SMMU).
- An optimized Custom Engine Interface (CEI)
- Up to three Coprocessor Interfaces (CI)
- A flexible Local Memory Interface (LMI) to cache, scratchpad RAM, or ROM.
- A Lexra Bus Controller (LBC) to connect peripheral functions and secondary memories to the processor s own local buses.

The following sections will discuss each of these system building block interfaces.

SMMU

The LX-4080 SMMU is designed for embedded applications using a single address space. Therefore, its primary function is to provide memory protection between user space and kernel space. The SMMU is compatible with the MIPS address space scheme for User/Kernel modes, mapping, and cached/uncached regions. The upper bits of the physical address can be ignored to form a smaller contiguous memory space.

LOCAL MEMORY INTERFACE

The LX-4080 s Harvard Architecture supports two LMI types: instruction memory and a data memory. Both memories use simple 32 bit synchronous RAM. The synchronous memory interface gives designers the fastest interface to memory blocks.

When used as a cache memory controller, the LMI includes a two-way set associative instruction cache interface and a write-through, direct mapped data cache interface. The tag compare logic as well as a cache replacement algorithm are provided as part of the LMI. One of the instruction cache sets can be locked down as un-swappable local memory.

In all cases, the LMI block is designed to easily interface with standard 32-bit wide memory blocks provided by ASIC vendors or by COT library vendors.

COPROCESSOR INTERFACE

Lexra supplies an optional Coprocessor Interface (CI) for applications requiring this functionality. Up to three CIs may be implemented in one design. The Coprocessor Interface "eavesdrops" on the Instruction. If a Coprocessor load (LWCz) or "move to" (MTCz, CTCz) is decoded, data will be enabled from the Data Bus into a CI register, then supplied to the designer-defined Coprocessor. Similarly, if a Coprocessor store (SWCz) or "move from" (MFCz,

CFCz) is decoded, data will be fetched from the Coprocessor and loaded into a CI register, then transferred onto the Data Bus in the following cycle. The design interface includes a variable-width data bus, five-bit address and independent read and write selects for Coprocessor registers and control registers. The LX-4080 pipeline and Harvard Architecture permit single cycle Coprocessor access and transfer. Designer-defined Coprocessor condition flags CpCondz are synchronized by the CI then passed to the Sequencer for testing in branch instructions.

CUSTOM ENGINE INTERFACE

The LX-4080 includes a Custom Engine Interface (CEI) which the designer can use to extend the MIPS ALU opcodes with application-specific or proprietary operations. Similar to the standard ALU, the CEI supplies the Custom Engine two input 32-bit operands, SRC1 and SRC2. One operand is selected from the Register File. Depending on the opcode, the second operand is either selected from the Register File or is a 16-bit sign-extended immediate. The opcode is locally decoded by the custom engine and, following execution by the custom engine, the result is returned on the 32-bit RES bus to the LX-4080. To support slower or multi-cycle operations, a stall signal is supplied by the interface. As an example, the MIPS MULT and DIV instructions are implemented as CEI functions, so designers without the need for multiply or divide do not have to pay the die size penalty.

LEXRA BUS CONTROLLER

The Lexra Bus Controller (LBC) is the interface between the LX-4080 and the outside world, which includes DRAM and various peripherals. It is a non-multiplexed, non-pipelined, and non-parity checked bus to provide the easiest bus protocol for design integration. On the processor side, the LBC provides a write-buffer of configurable depth to support the write-through cache, as well as the control for byte and half-word transfers. On the peripheral side, LBC is designed to easily interface to industry standard bus protocols, such as PCI, USB and FireWire.

From the silicon implementation standpoint, the LBC can run either asynchronously at any speed from 33 MHz all the way to the speed of the processor core, or synchronously with the CPU to maximize the system throughput.

BUILDING BLOCK INTEGRATION

Several steps have been taken to minimize the time and effort to integrate the LMI, CI, CEI, and LBC. First, a LX-4080 configuration software tool provides a menu of selections for designers to specify building blocks needed, number of different memory blocks, target speed, target cell library, etc. Then the configuration software automatically generates a reference LX-4080 top level Verilog model, makefiles, and scripts for different steps of the supported design flow.

For testability purpose, all building blocks contain scan control signals. These signals can be gathered at the system level, and multiplexed for the DFT software to sequentially test each building block.

SOFTWARE TOOL SUPPORT

The Lexra Software Developers' Kit (LSDK) allows designers to develop software targeted designs incorporating the Lexra LX-4080. The LSDK is built around the GNU Tools environment enabling software development using the C, C++, and MIPS assembly programming languages. These tools include the GNU compiler, assembler, linker, library archive utility, and debugger. Programs developed in this environment can be loaded and run with a Verilog simulation model or the actual LX-4080. The LSDK also includes source code for the GNU tools to allow further customization to suit designer enhancements to the LX-4080.

In addition, the LSDK also includes PMON, "The MIPS Family Prom Monitor". PMON is a public domain debug monitor that is designed to assist programmers of MIPS-based embedded systems to initialize the system, test, and debug their software.

Finally, the LSDK includes a simple Standard C and math library for the GNU C environment. It has been developed for use by embedded applications, and contains enhancements for exception handling that are optimized for the LX-4080.

EVALUATION SYSTEM BOARD (ESB)

The ESB is a PCI card based evaluation board supporting both hardware prototyping as well as software development. The ESB includes a LX-4080 test chip, up to 32 MB of DRAM, serial link to Sun workstation, as well as connection to the PCI motherboard. The test chip interface brings out the CEI, CI and LBC pins for designers to prototype system level hardware logic.

EDA TOOL SUPPORT

Lexra intends to support all popular EDA software, so designers do not have to alter their design methodology. For example, the LX-4080 fully supports .SDF timing backannotation to simulation and timing analysis tools. The following is a snapshot of EDA tools currently supported:

Design Flow	Tools Supported
Simulation	VCS
Synthesis	Design Compiler
Static Timing	Motive, PrimeTime
DFT	Sunrise
P&R	Aquarius/XO

REFERENCE SPECIFICATION

The exact performance of the LX-4080 depends upon the silicon process and the implementation technology used. Furthermore, this specification depends on the memory configuration and CI/CEI selection. The following reference SmoothCore specification for the processor core itself is based upon UMC s 0.35 μ salicide process.

Specification (CPU only)	LX-4080
Transistor count	86,000
Die size (mm2)	1.8
Frequency (worst case MHz)	100
Power dissipation (mW)	150
Operating voltage (V)	3.3
Operating environment	WC Commercial

For more information, contact Lexra at (781) 899 5799, or visit the Web site at http://www.lexra.com

*MIPS unaligned load and store instructions are only supported through software emulation